

FIG. 1

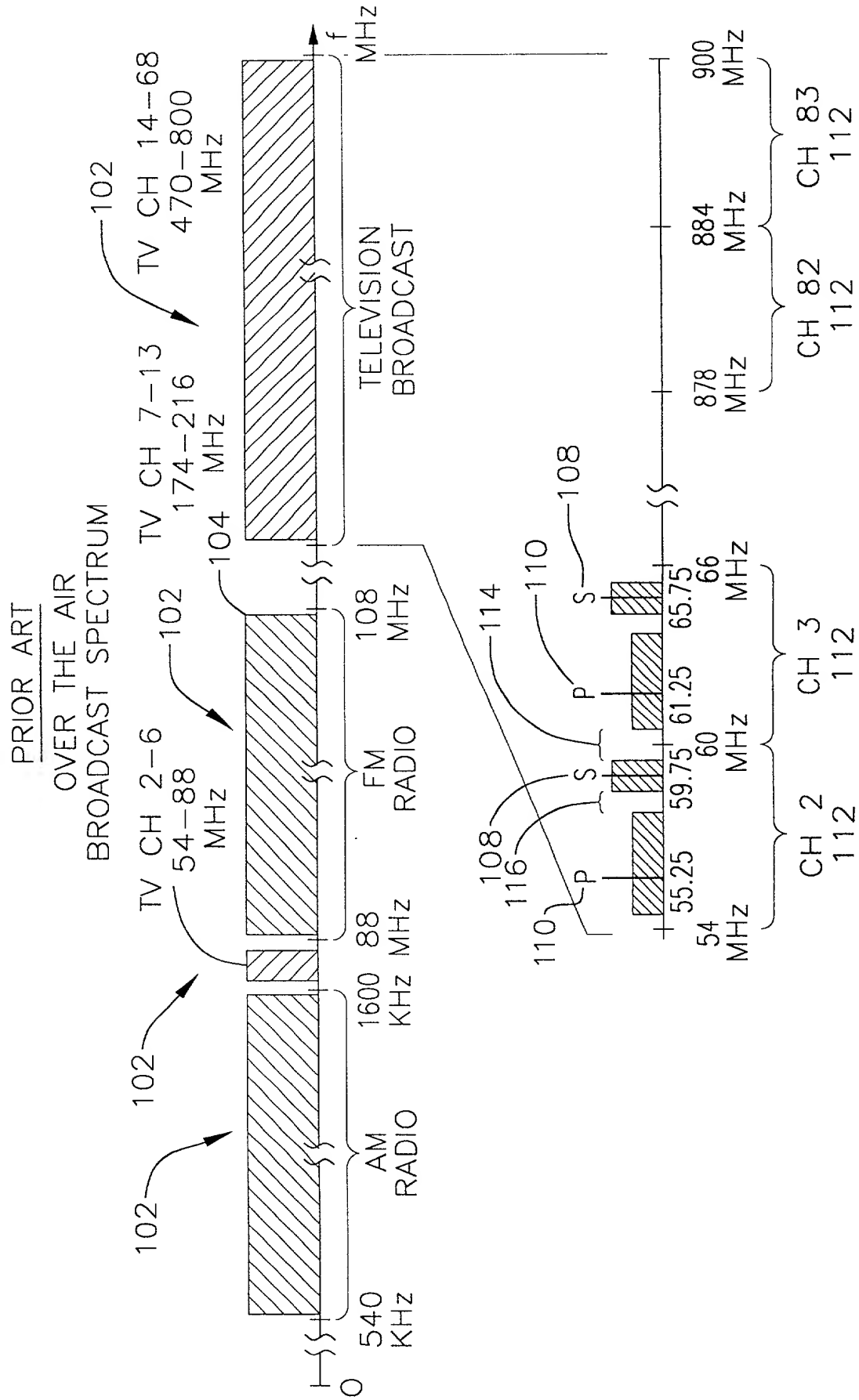


FIG. 2

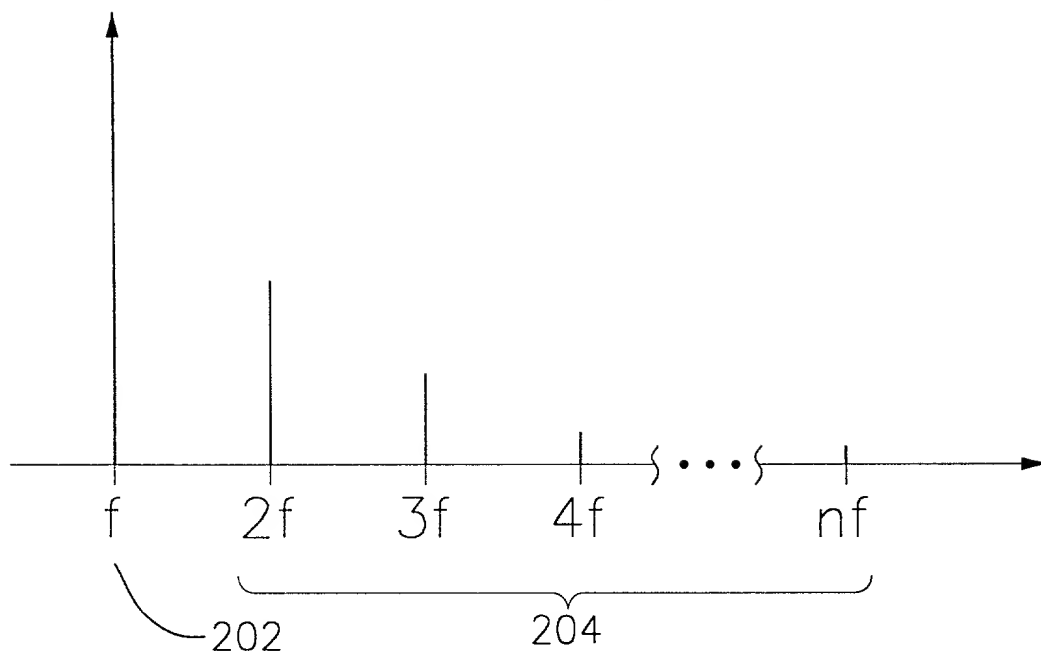


FIG. 3
PRIOR ART

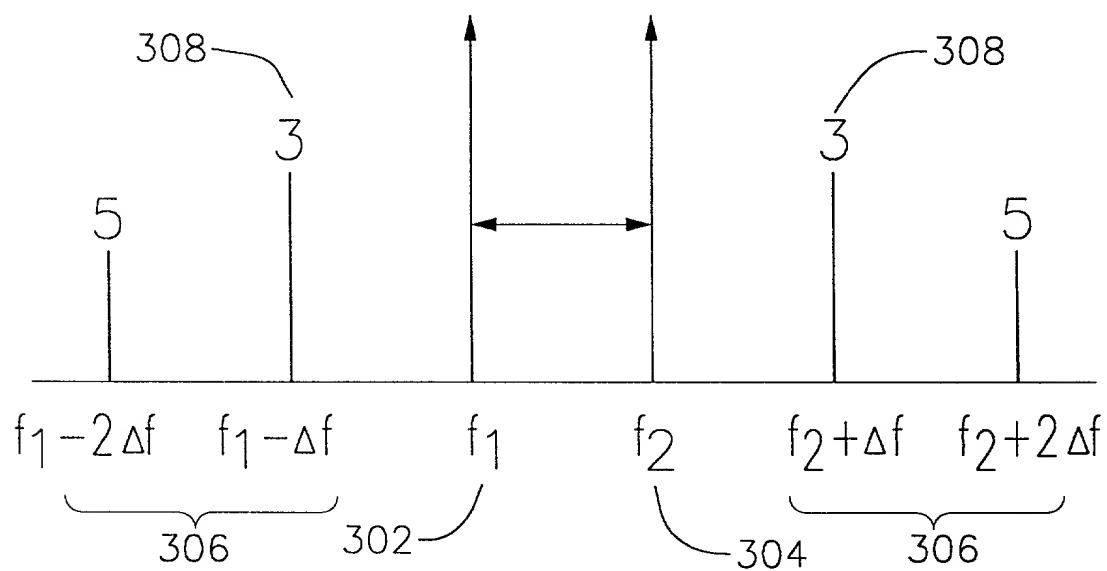


FIG. 4

PRIOR ART

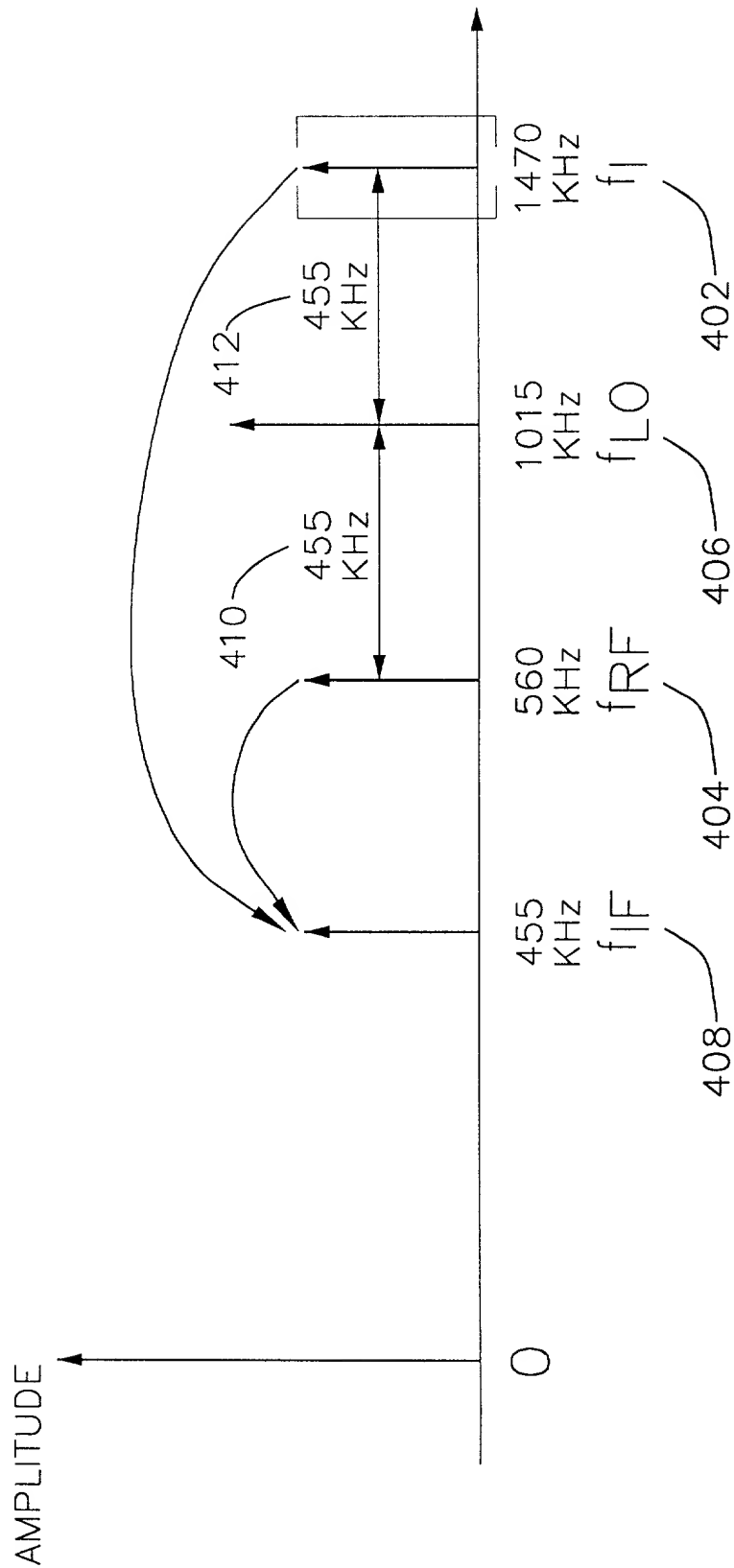


FIG. 5

DUAL CONVERSION RECEIVER

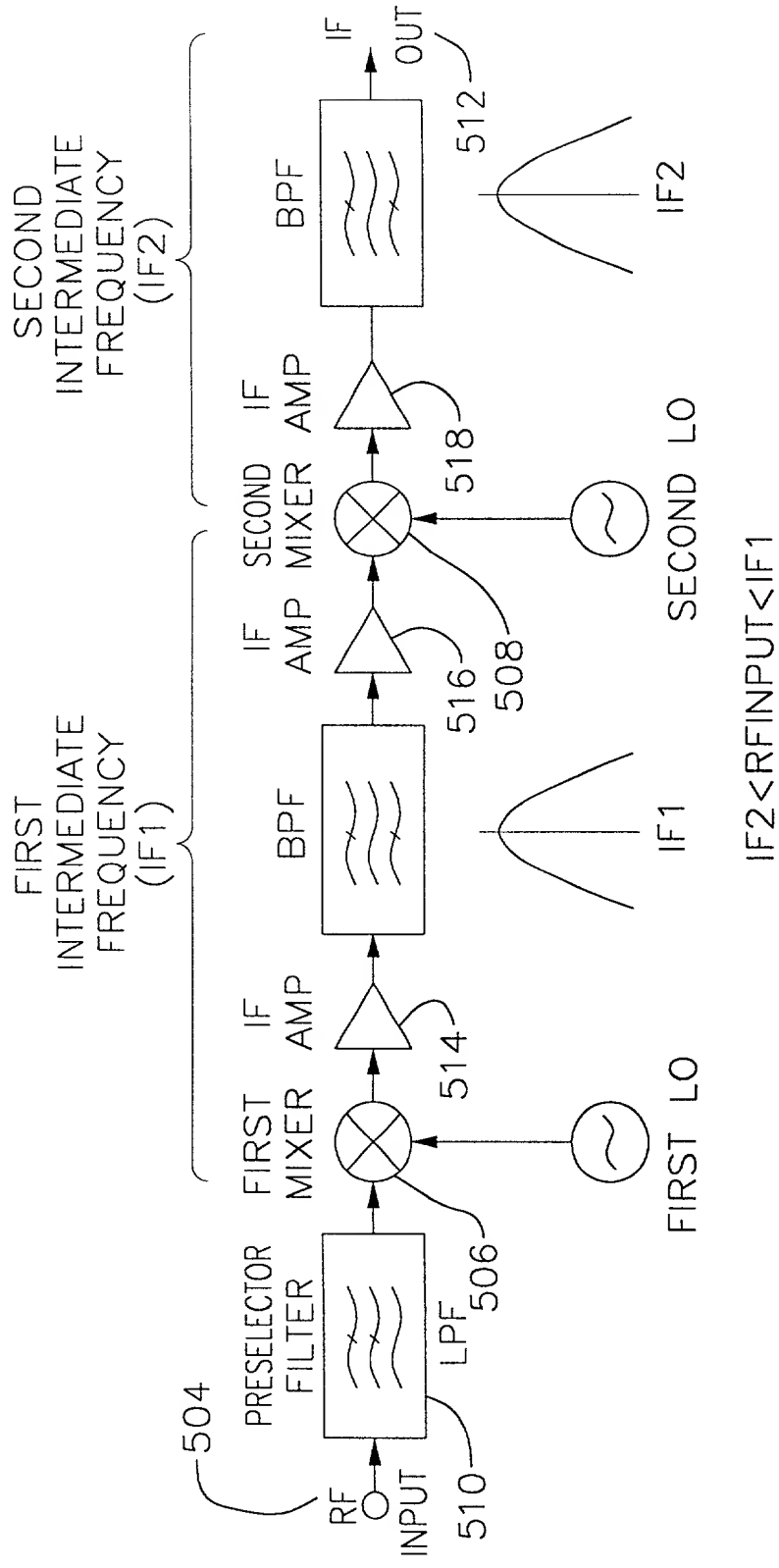


FIG. 6

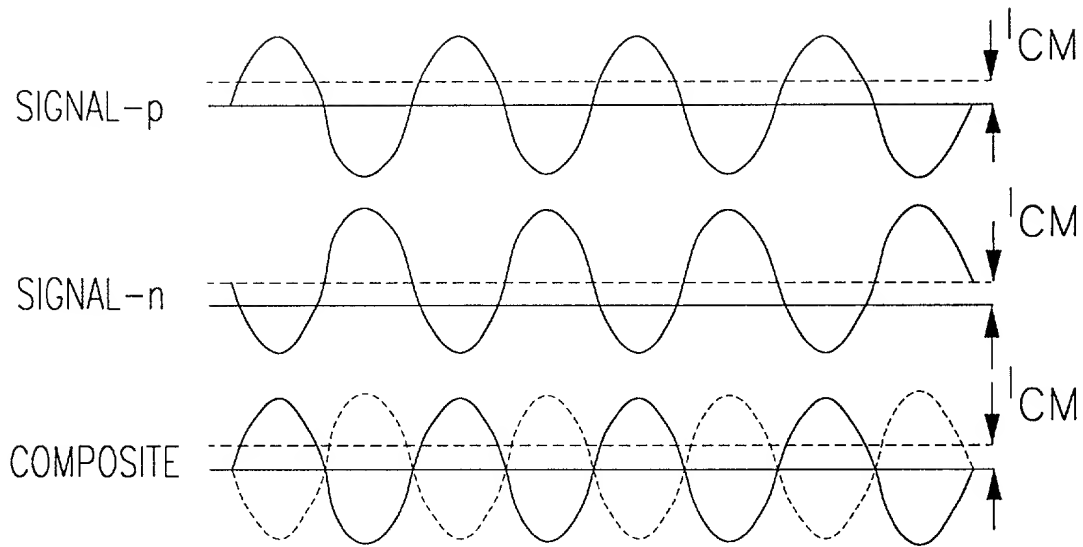


FIG. 7

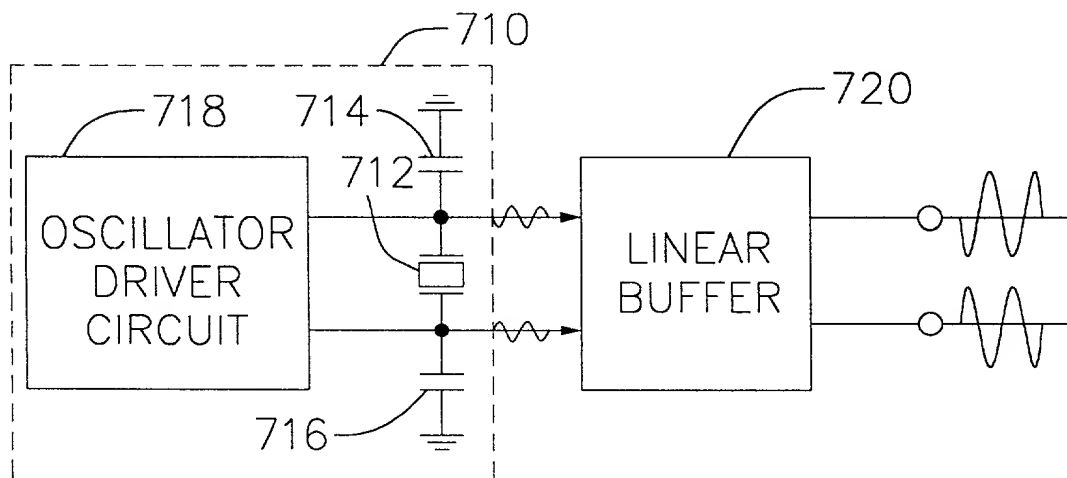


FIG. 8

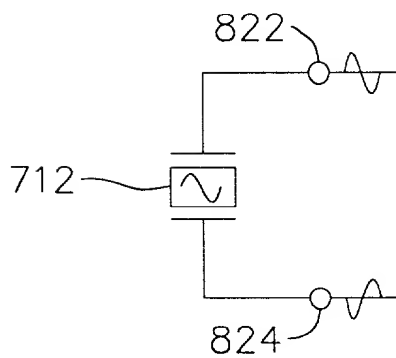


FIG. 9

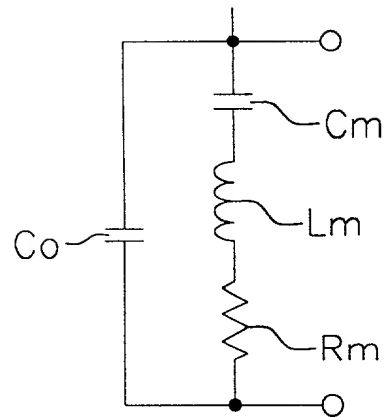


FIG. 10

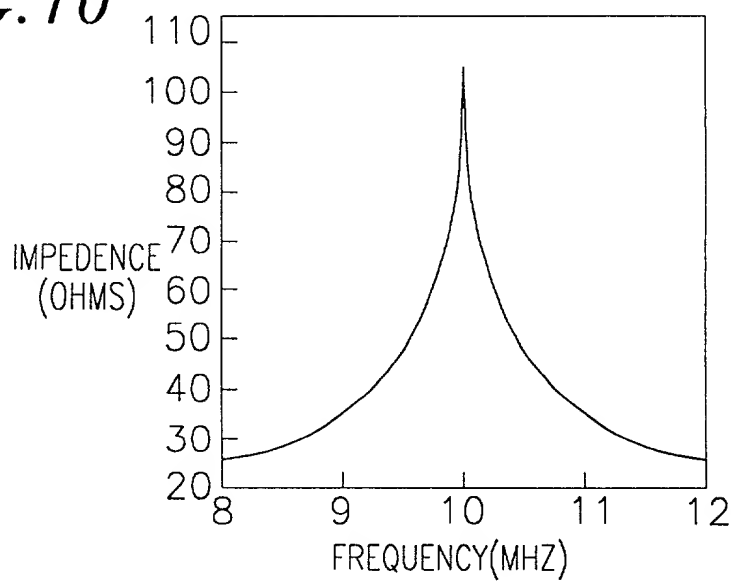


FIG. 11

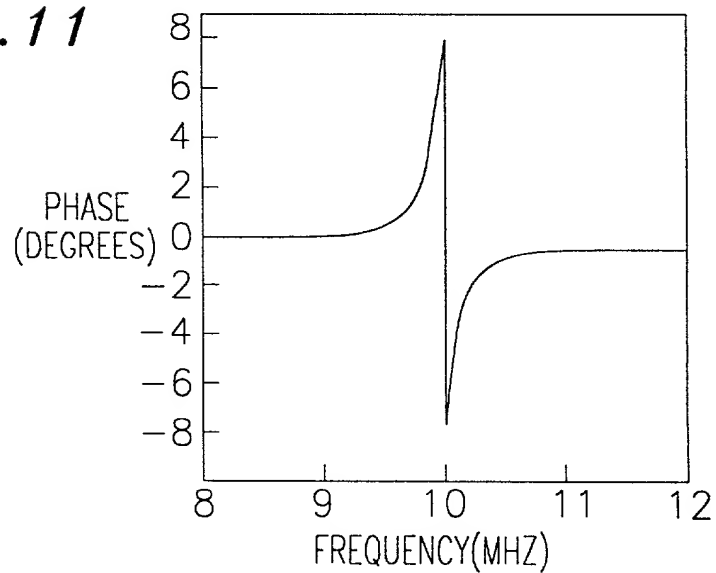


FIG. 12

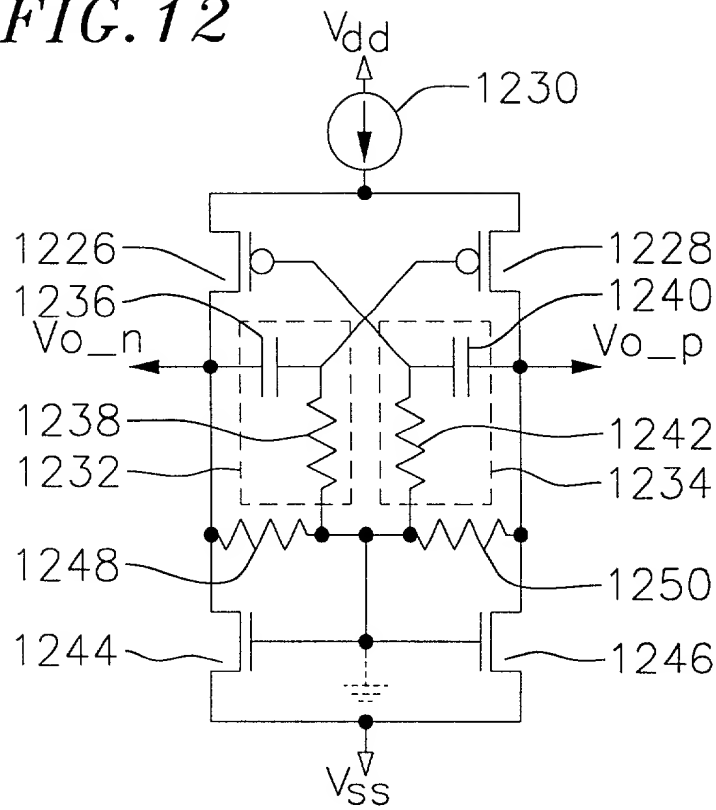


FIG. 13

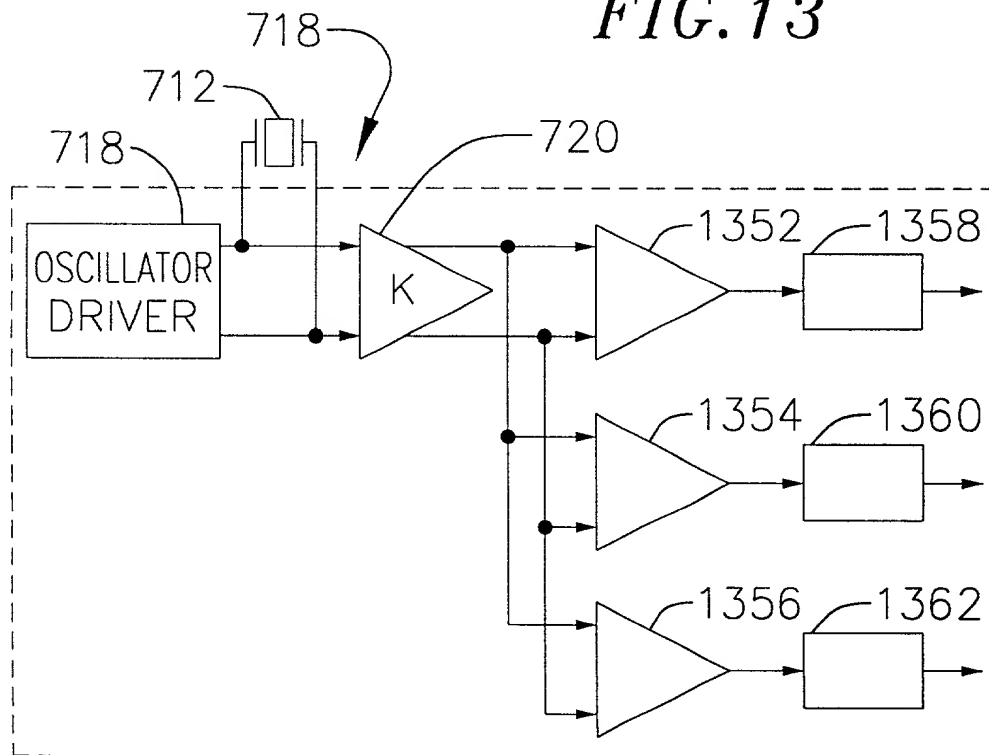


FIG. 14

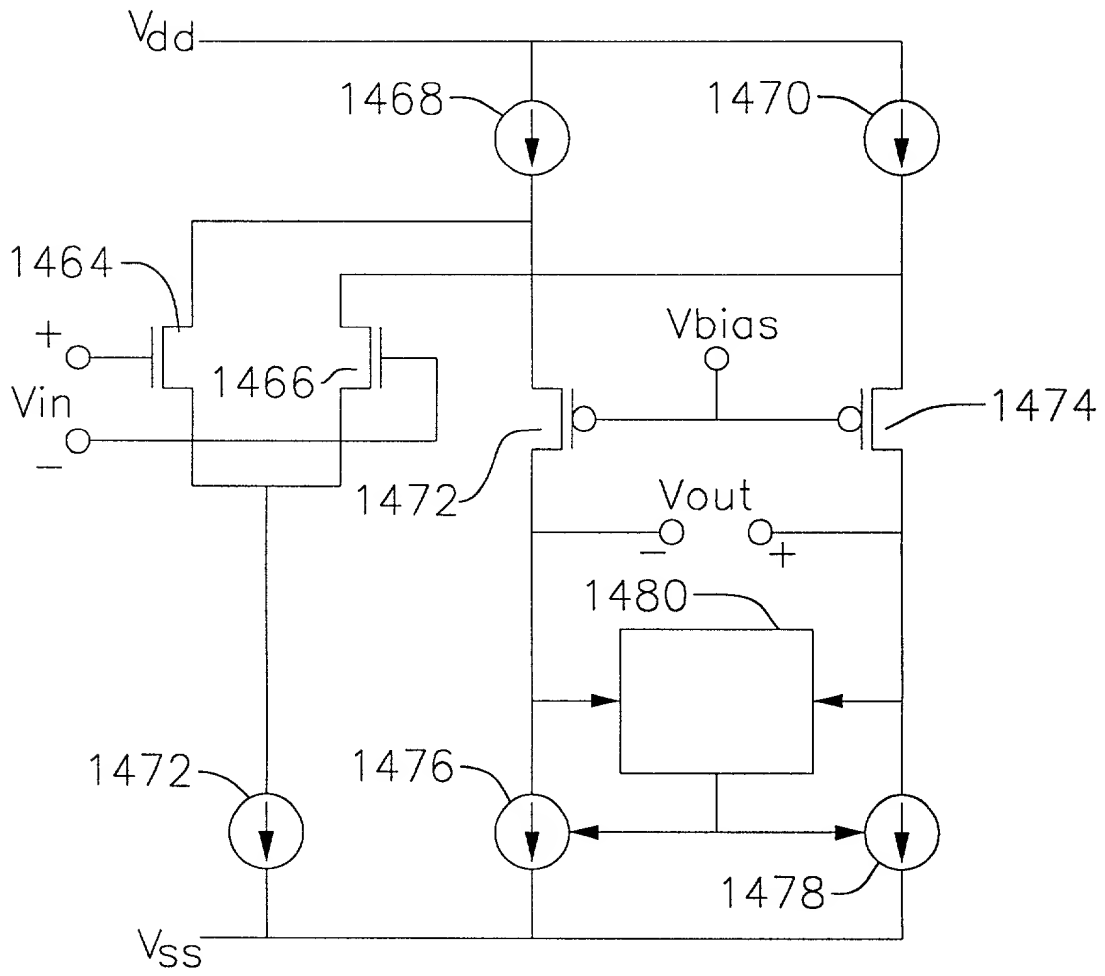


FIG. 15

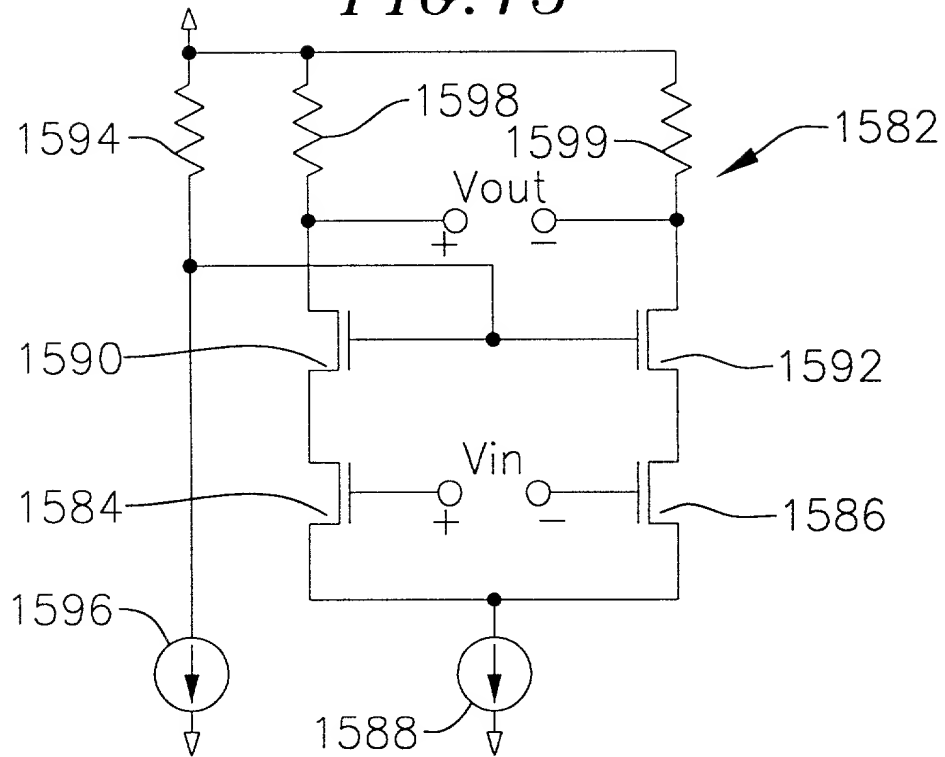


FIG. 16

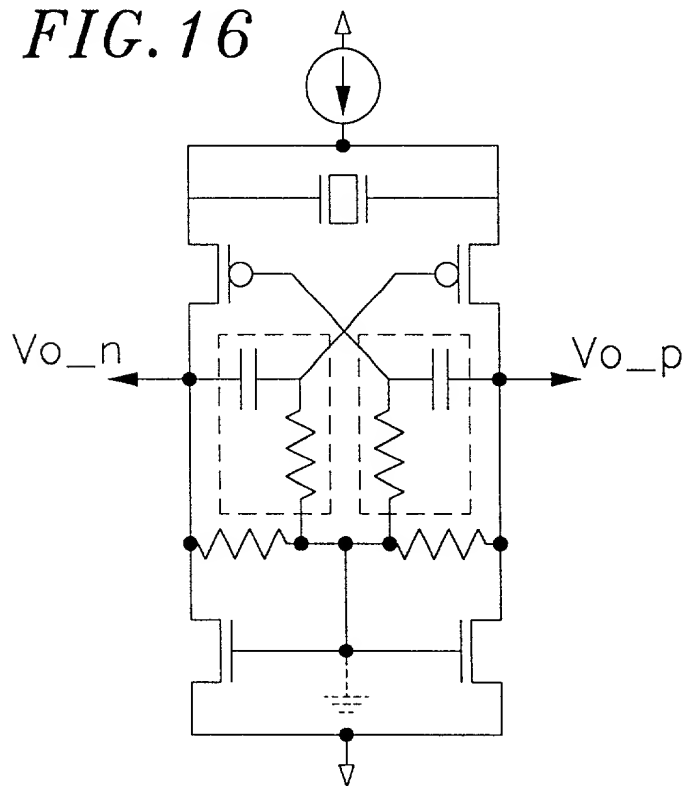


FIG. 17

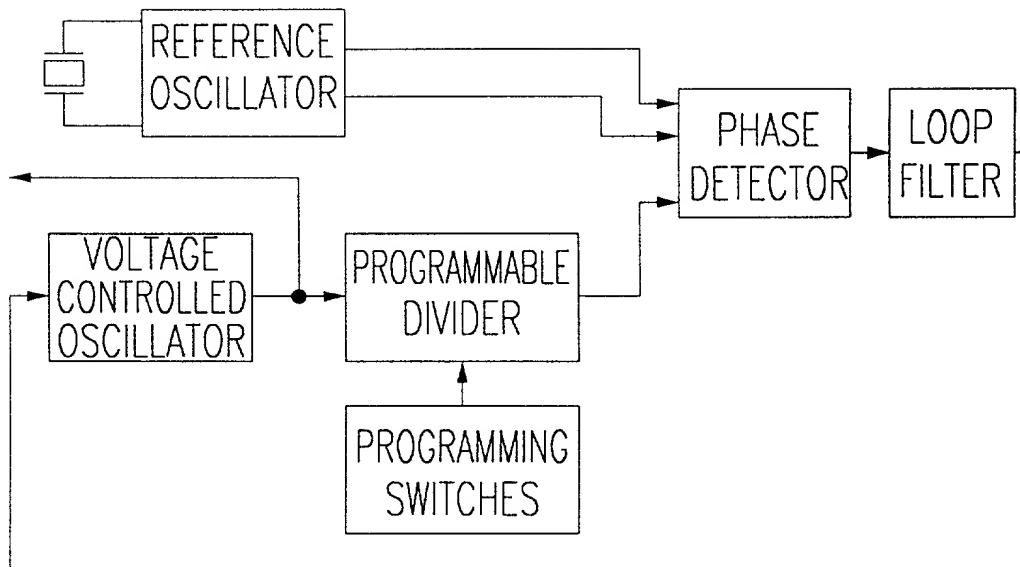


FIG. 18

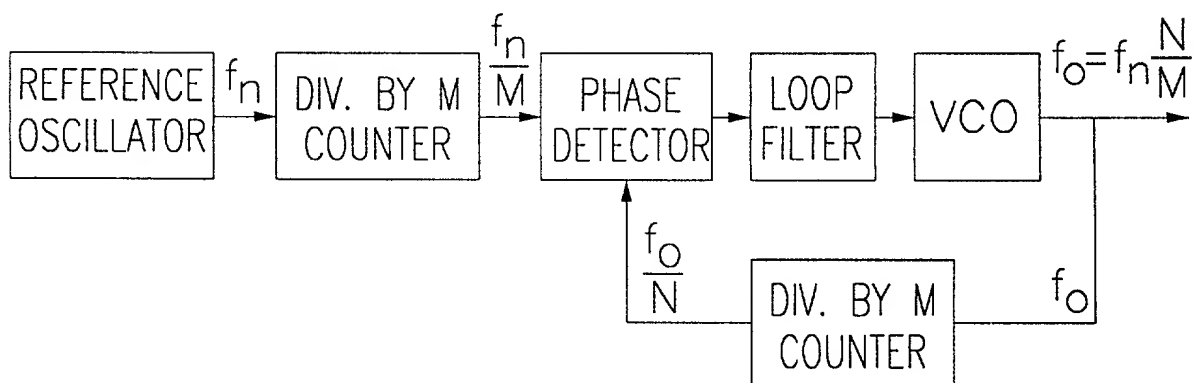


FIG. 19

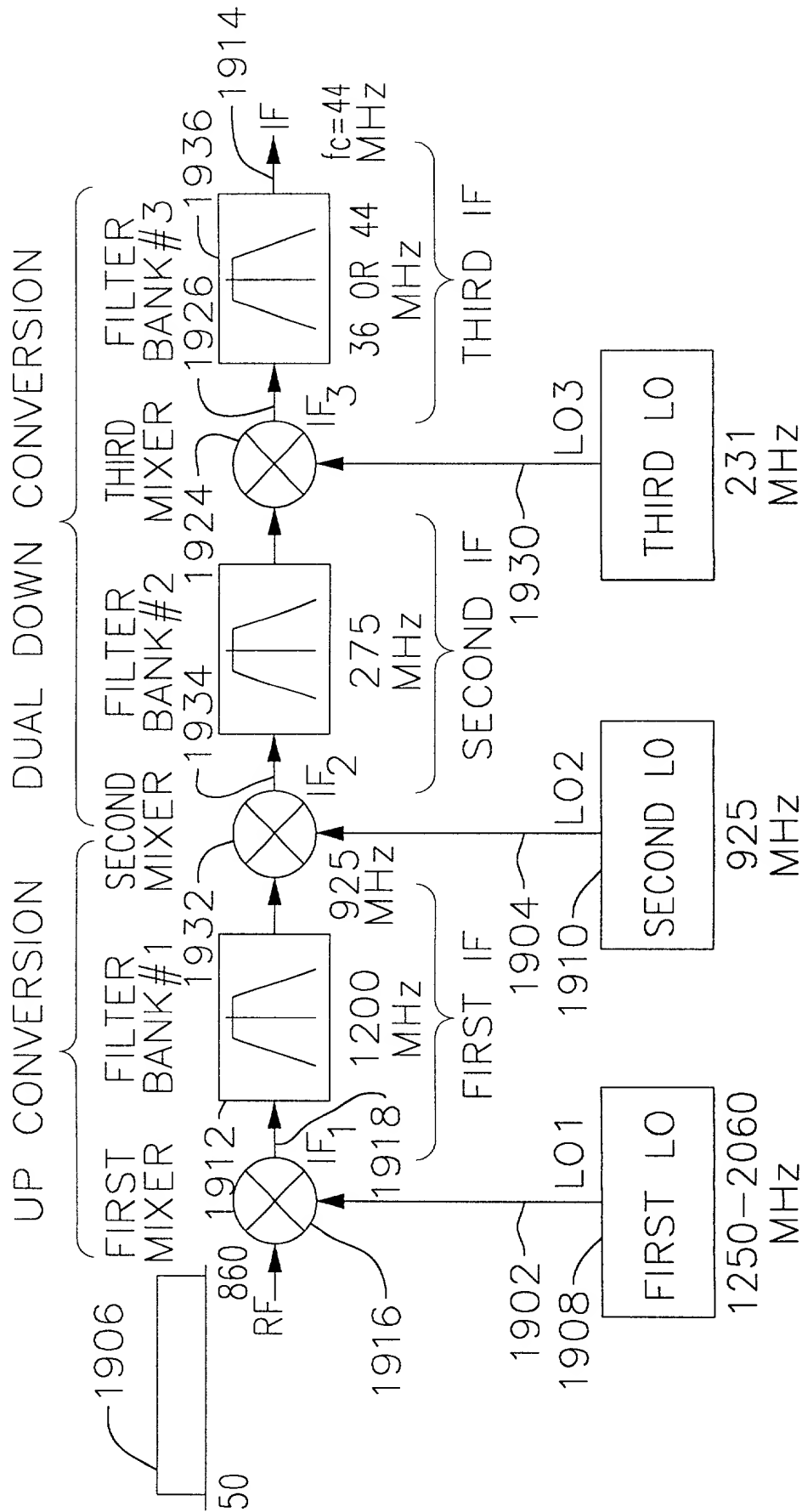
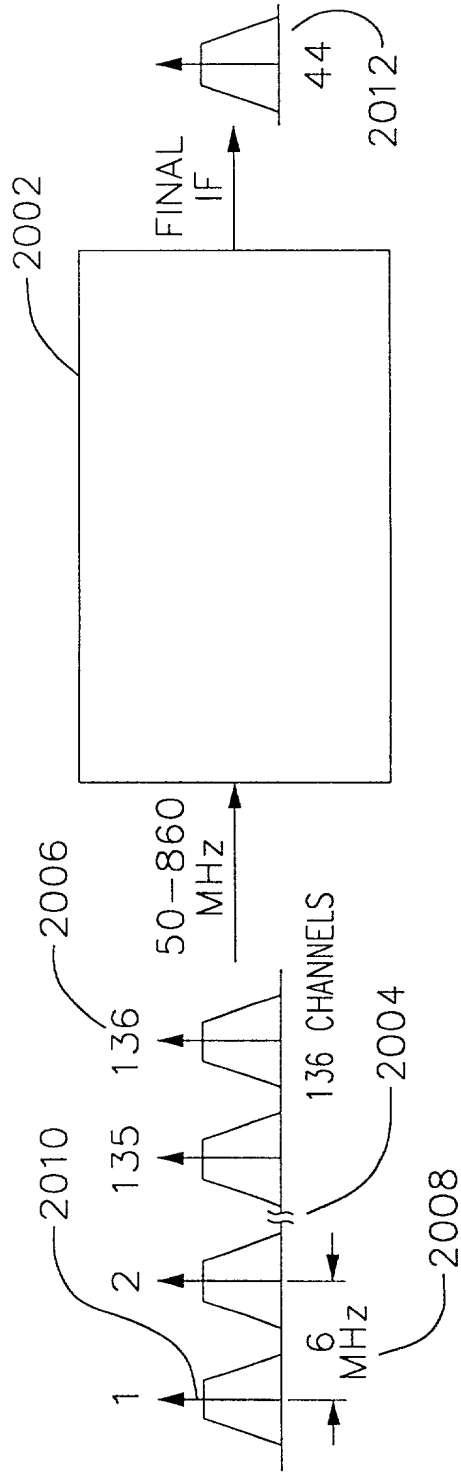


FIG. 20



PPL Xtal REFERENCE=10MHz
 LO-1, 10MHz FREQUENCY STEPS
 LO-2, 100kHz FREQUENCY STEPS

FIG.21

44MHz IF

TABLE OF FREQUENCIES BASED ON
 COARSE/FINE PLL SOLUTION:

NOTE
 • LO-2 REF=100KHz
 SO DIVIDE RANGE=9216 TO 9280

Frf (MHz)	50	56	62	68	74	80	86	92	98	104	110	116	122	128	"	854	860
LO-1 (MHz)	1250	1260	1260	1270	1270	1280	1290	1290	1300	1300	1310	1320	1320	1330	"	2050	2060
IF-1 (MHz)	1200	1204	1198	1202	1196	1200	1204	1198	1202	1196	1200	1204	1198	1202	"	1196	1200
LO-2 (MHz)	924.8	928.0	923.2	926.4	921.6	924.8	928.0	923.2	926.4	921.6	924.8	928.0	923.2	926.4	"	921.6	924.8
IF-2 (MHz)	275.2	276	274.8	275.6	274.4	275.2	276.0	274.8	275.6	274.4	275.2	276.0	274.8	275.6	"	274.4	275.2
LO-3 (MHz)	231.2	232	230.8	232	230	231	232	231	232	230	231	232	231	232	"	230	231
IF-3 (MHz)	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	"	44.0	44.0

PPL Xtal REFERENCE=10MHz
 LO-1, 10MHz FREQUENCY STEPS
 LO-2, 100kHz FREQUENCY STEPS

FIG. 22

36MHz IF

TABLE OF FREQUENCIES BASED ON
 COARSE/FINE PLL SOLUTION:

NOTE

- LO-2 REF=100KHz
 SO DIVIDE RANGE=9280 TO 9340

Frf (MHz)	50	58	66	74	82	90	98	106	114	122	130	138	146	154	"	852	860
LO-1 (MHz)	1250	1260	1270	1270	1280	1290	1300	1310	1310	1320	1330	1340	1350	1350	"	2050	2060
IF-1 (MHz)	1200	1202	1204	1196	1198	1200	1202	1204	1196	1198	1200	1202	1204	1196	"	1198	1200
LO-2 (MHz)	931.2	932.8	934.4	928.0	930	931	933	934	928.0	930	931	933	934	928.0	"	929.60	931.2
IF-2 (MHz)	268.8	269.2	269.6	268.0	268.4	268.8	269.2	269.6	268.0	268.4	268.8	269.2	269.6	268.0	"	268.4	268.8
LO-3 (MHz)	232.8	233.2	233.6	232	232	233	233	234	232	232	233	233	234	232.0	"	232.4	232.8
IF-3 (MHz)	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	"	36.0	36.0

FIG. 23

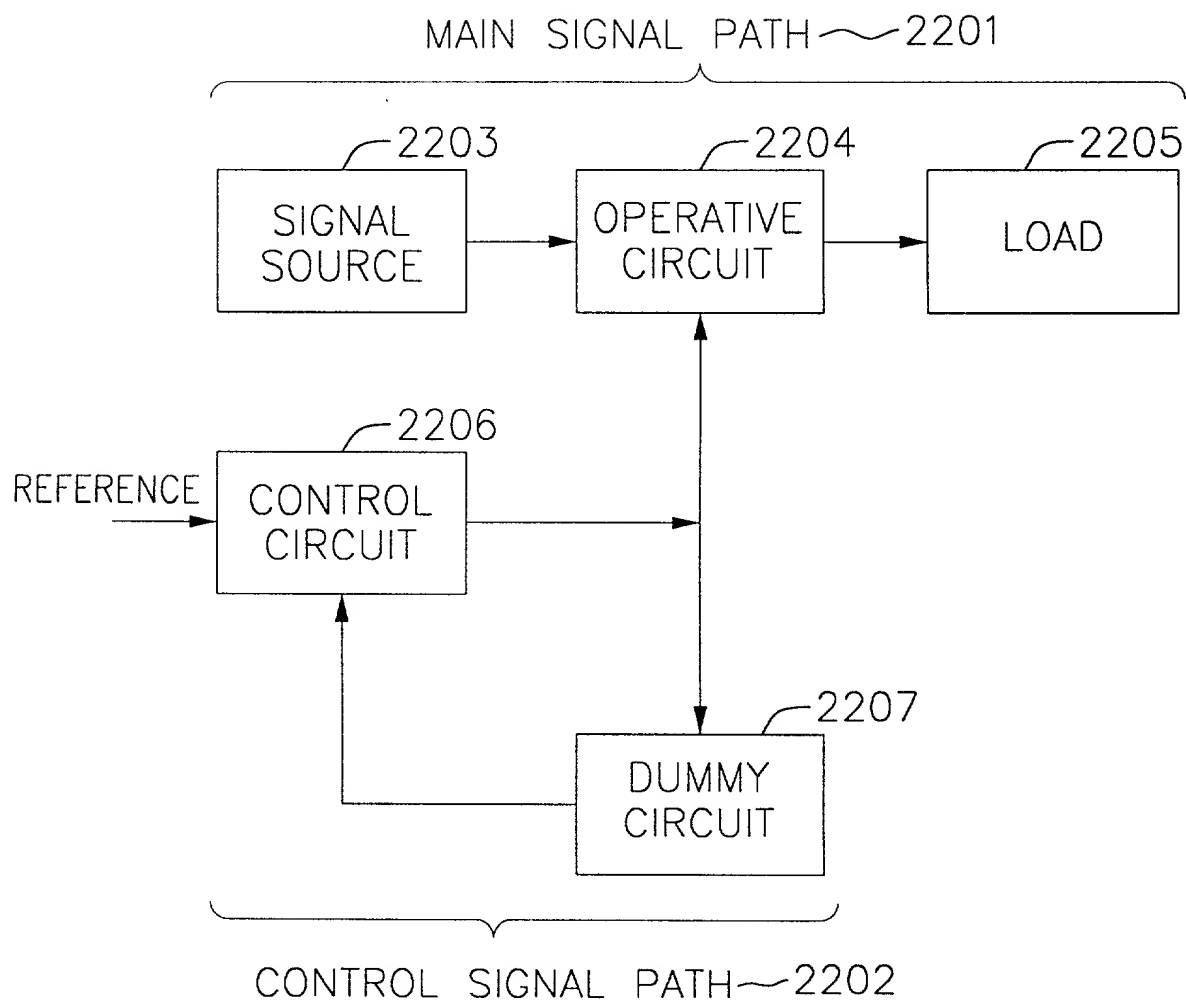


FIG. 24a

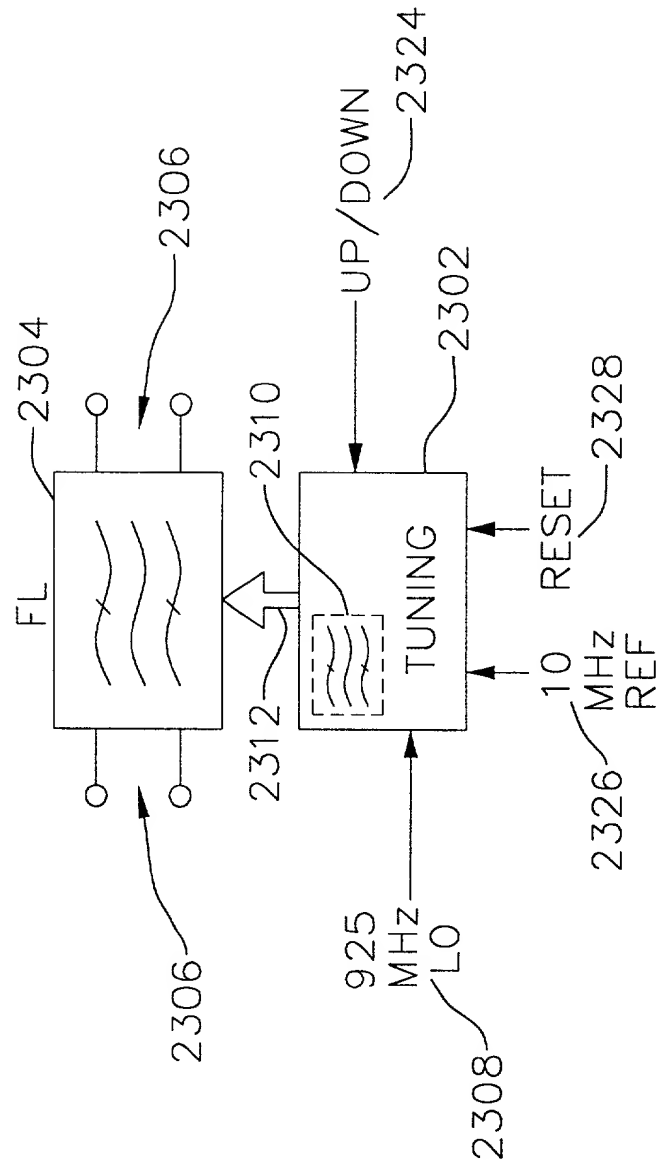


FIG. 24b

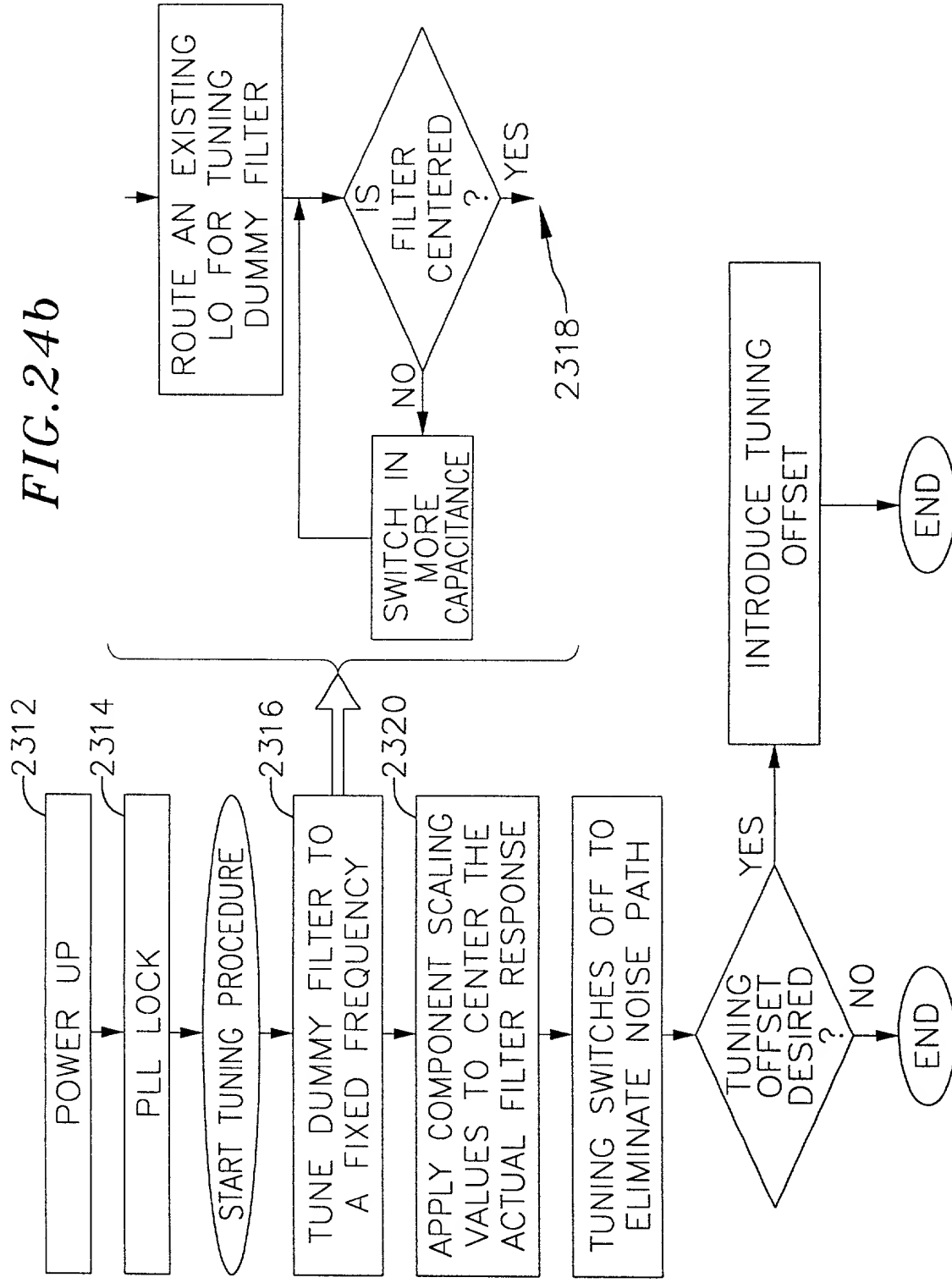


FIG. 24c

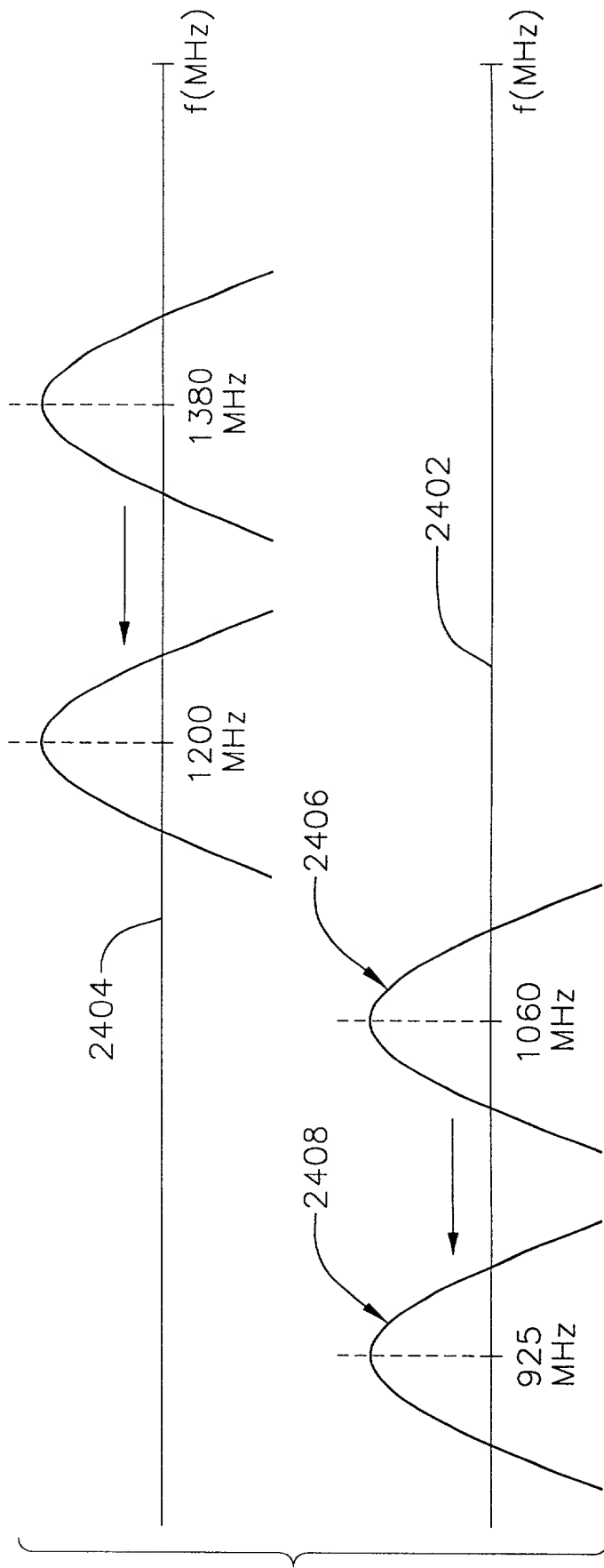


FIG. 25

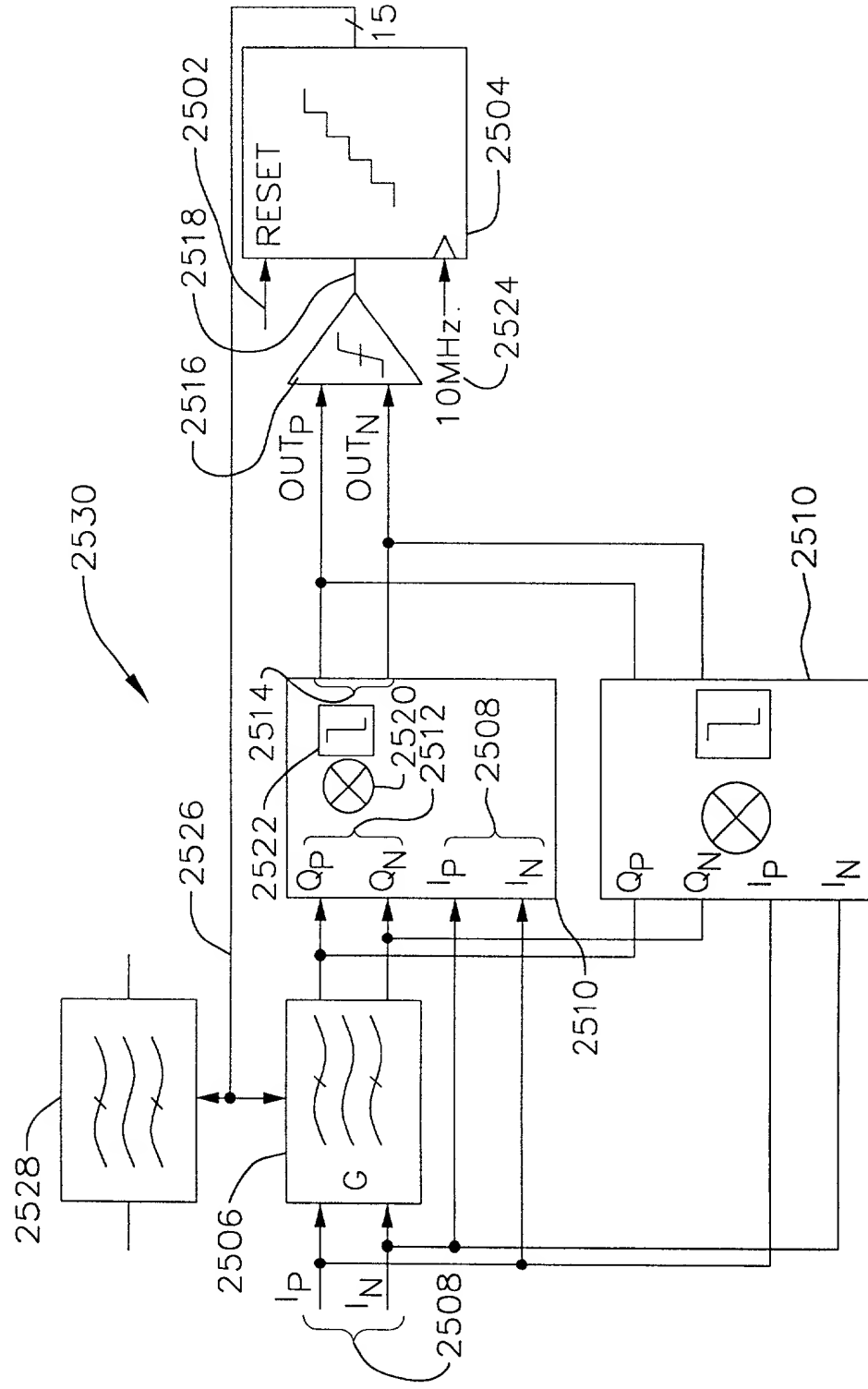


FIG. 26

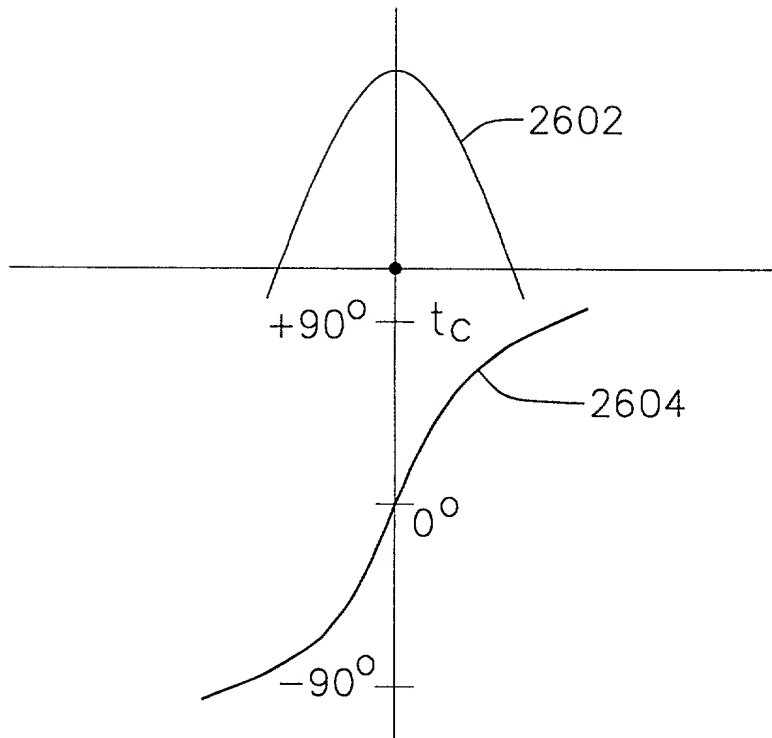
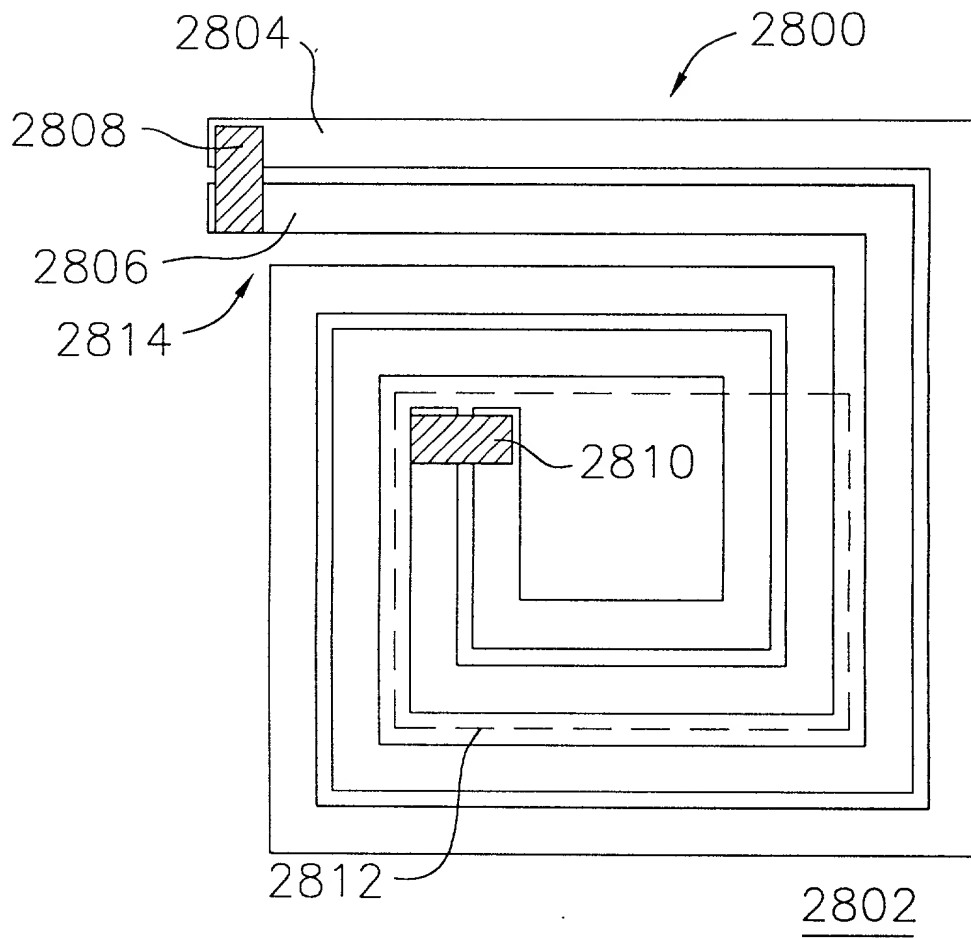




FIG.28a



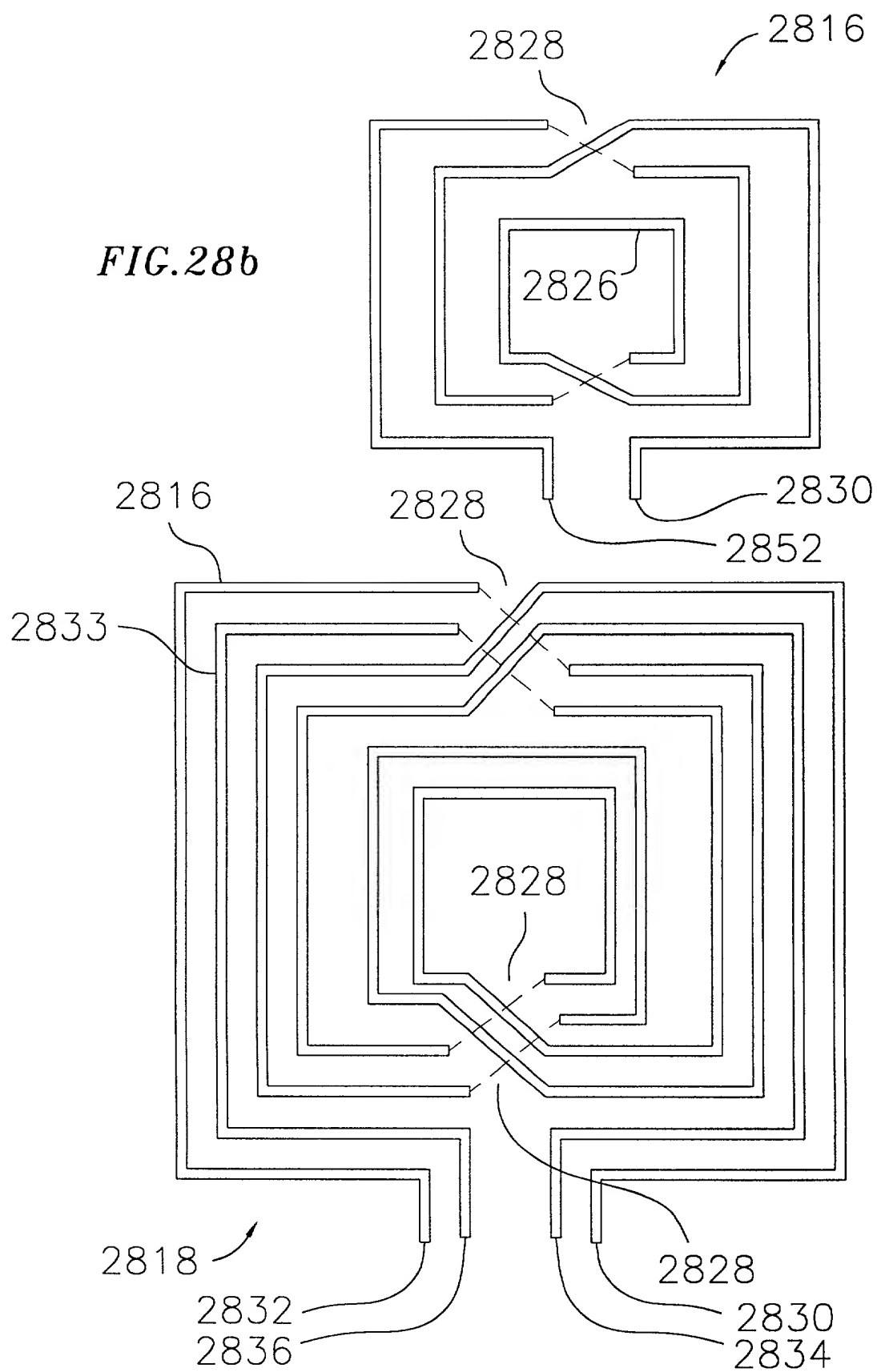
[illegible]

FIG. 28c

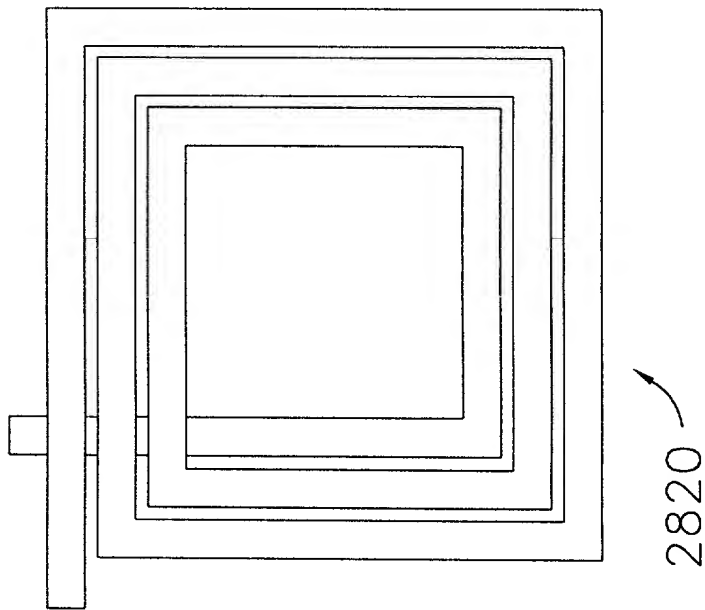


FIG. 28d

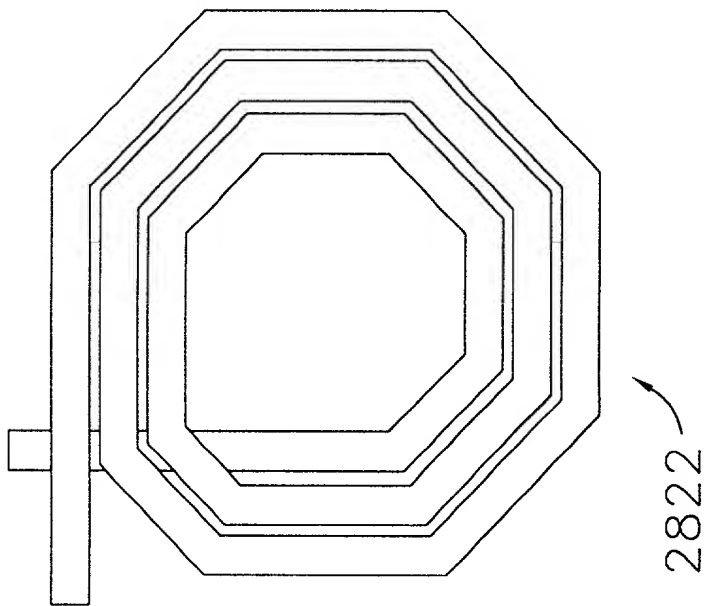


FIG. 28e

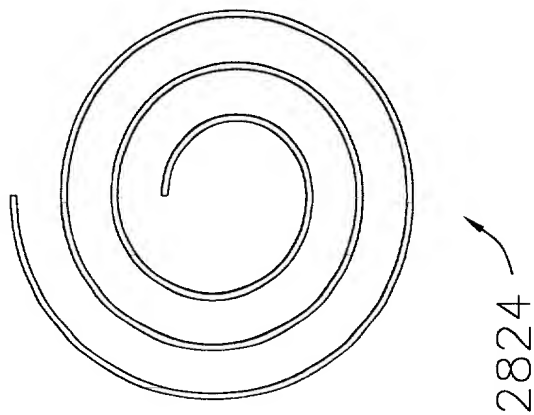


FIG.28f

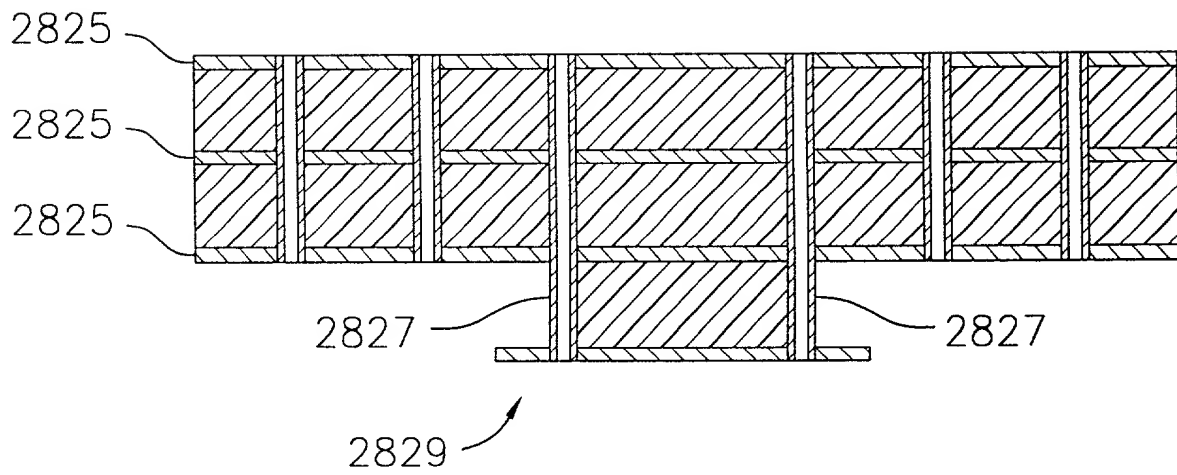


FIG.28g

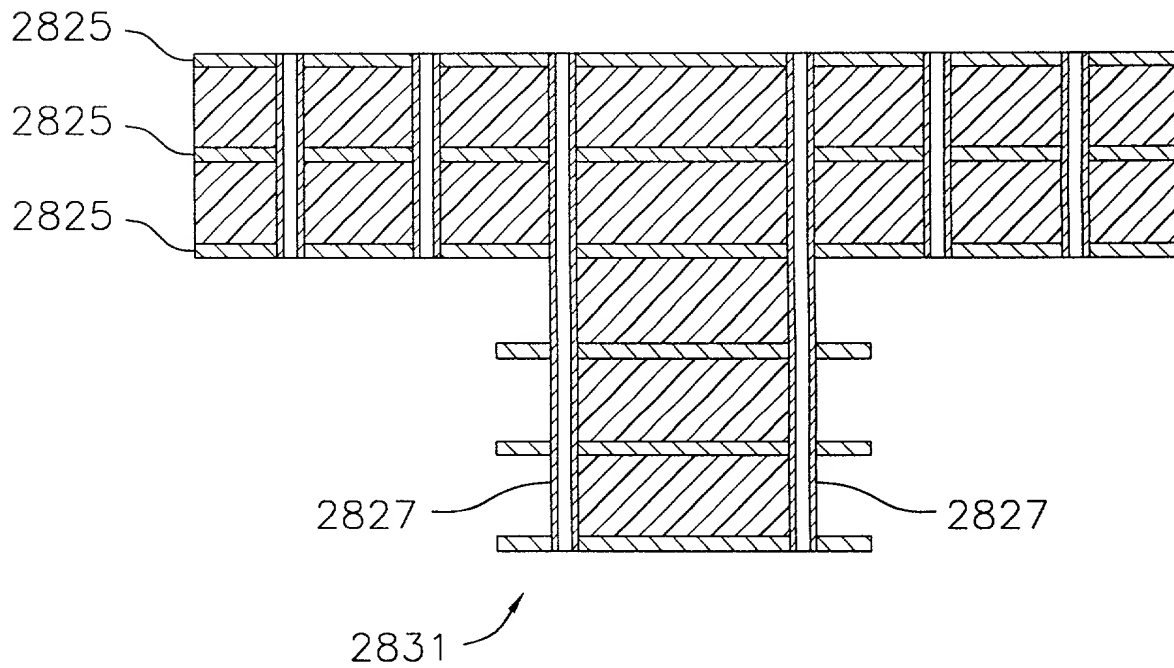


FIG.28h

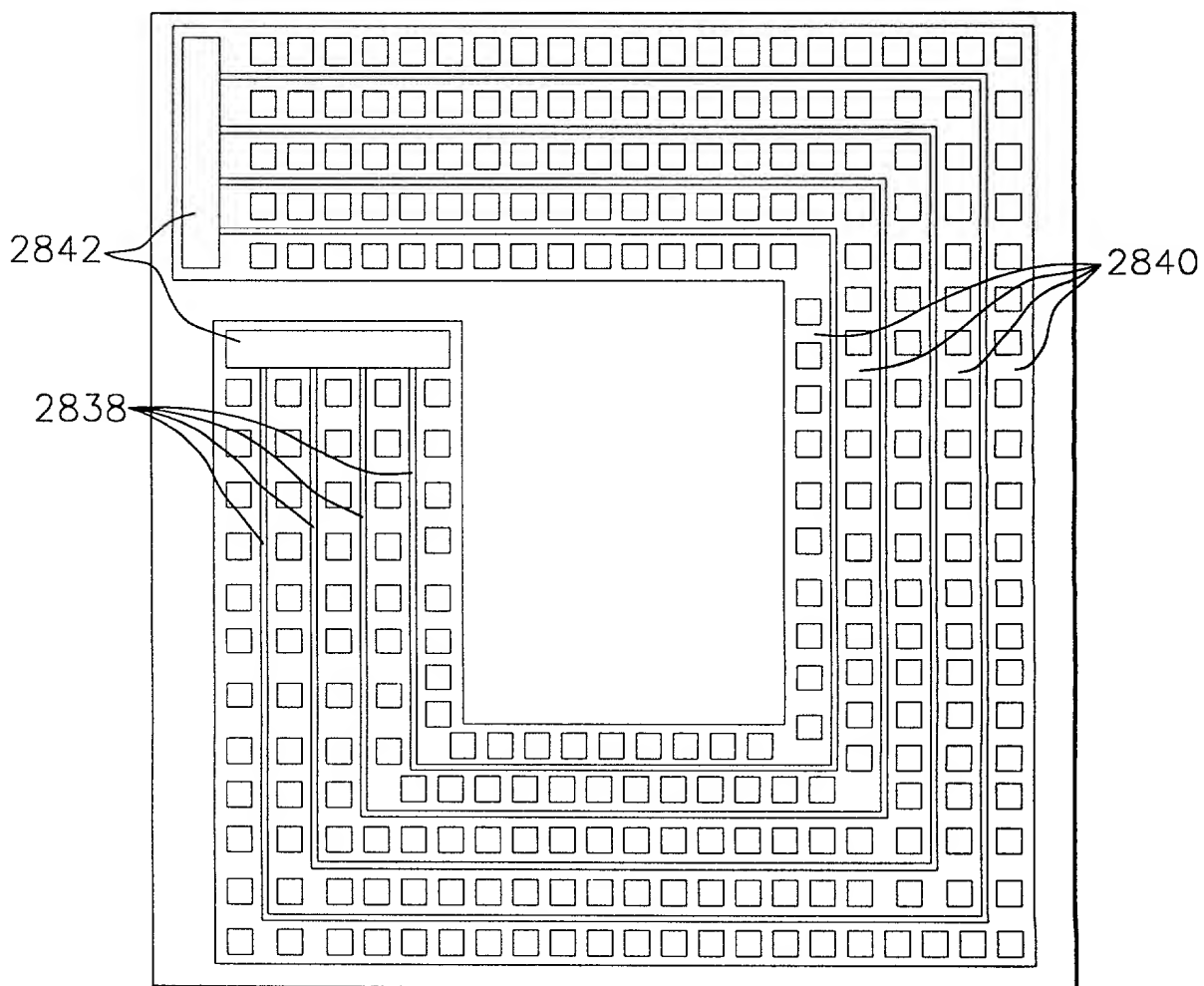


FIG. 28i

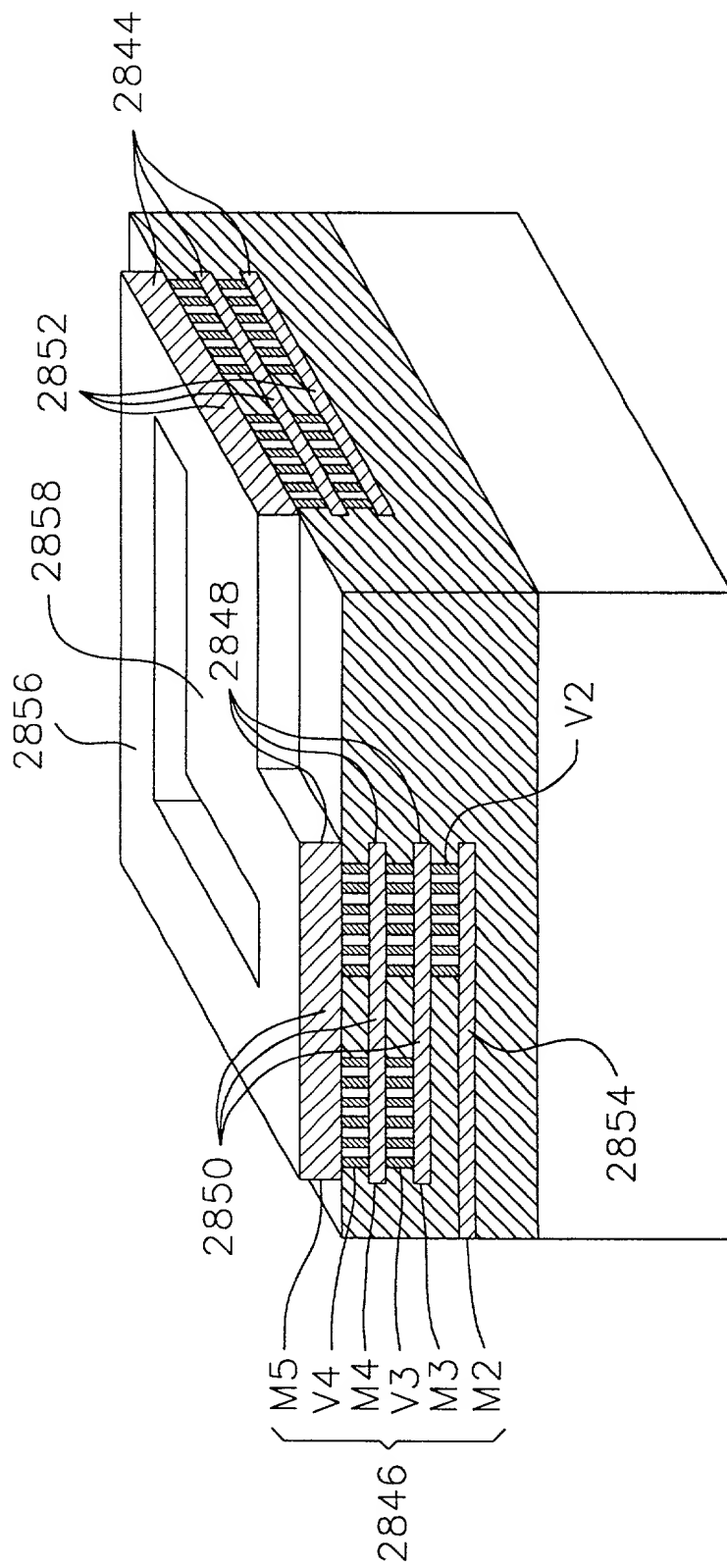


FIG. 28j

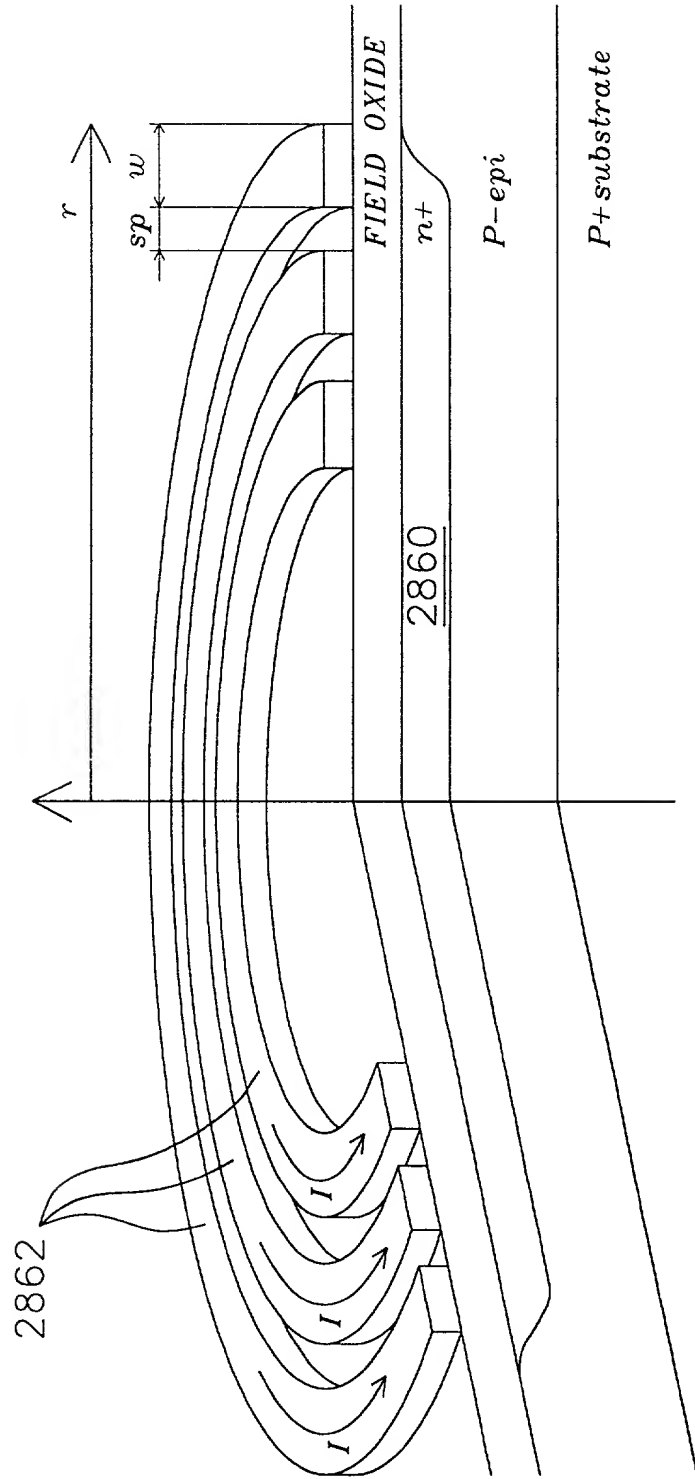


FIG. 28k

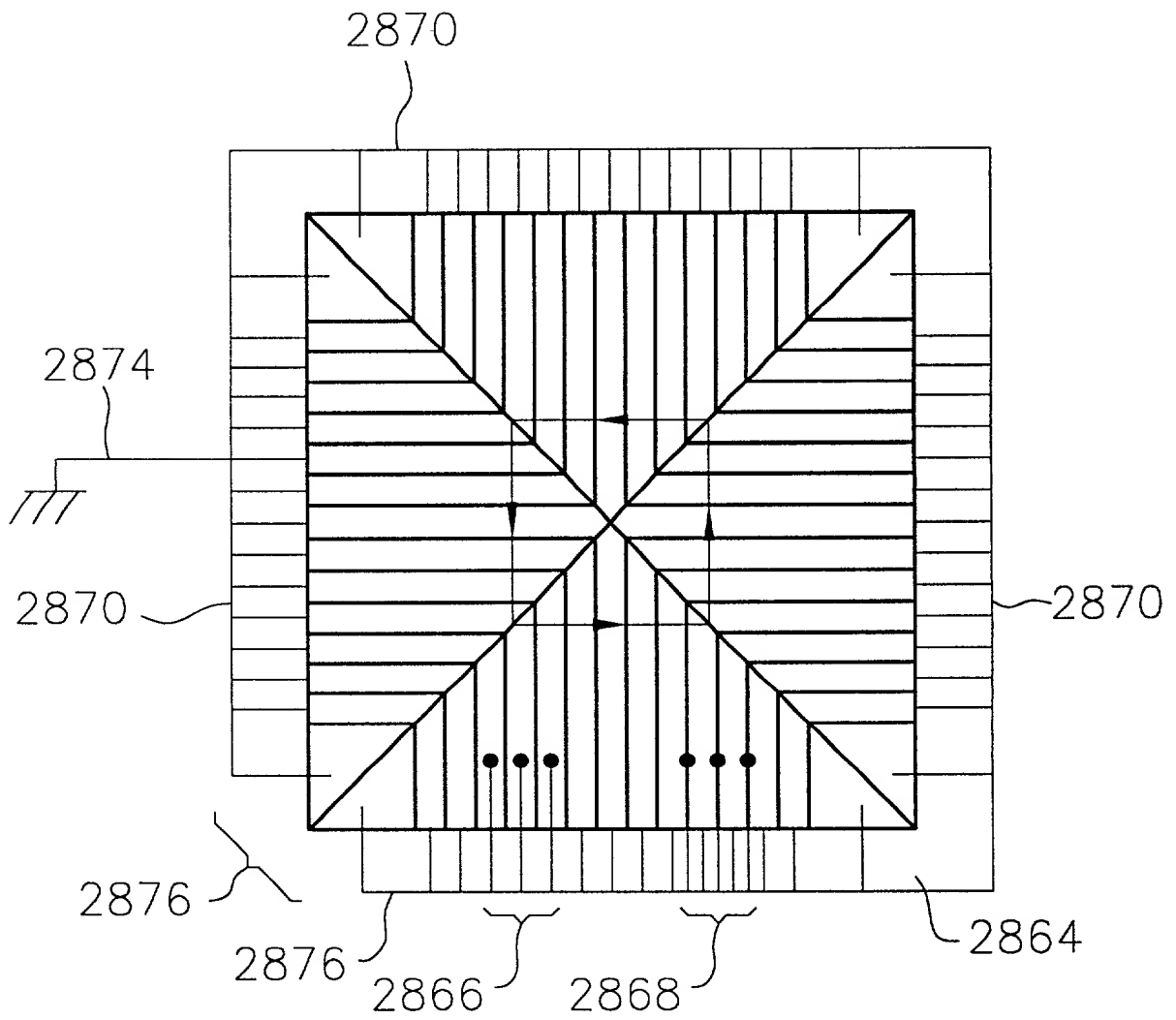


FIG.29

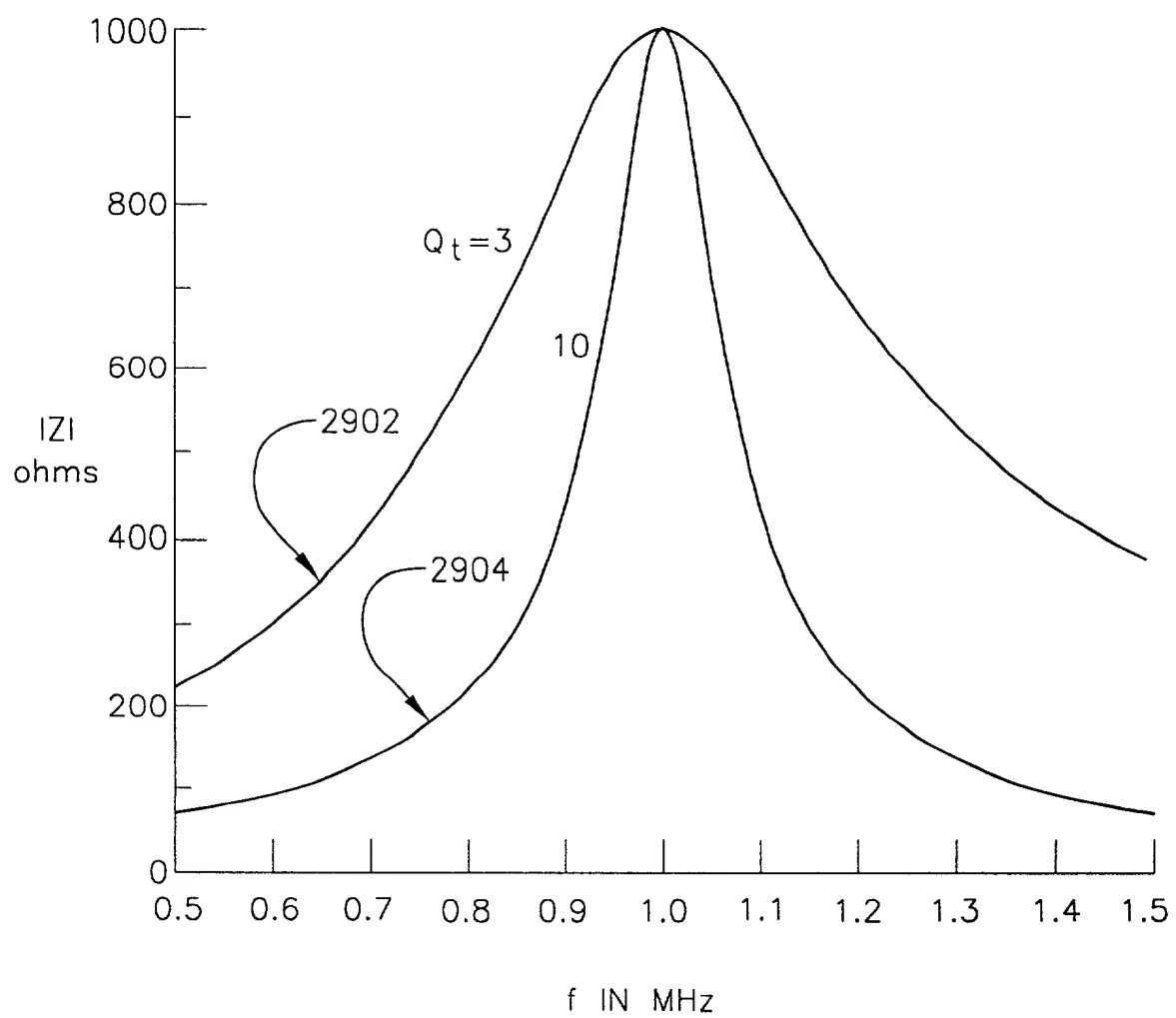


FIG. 30

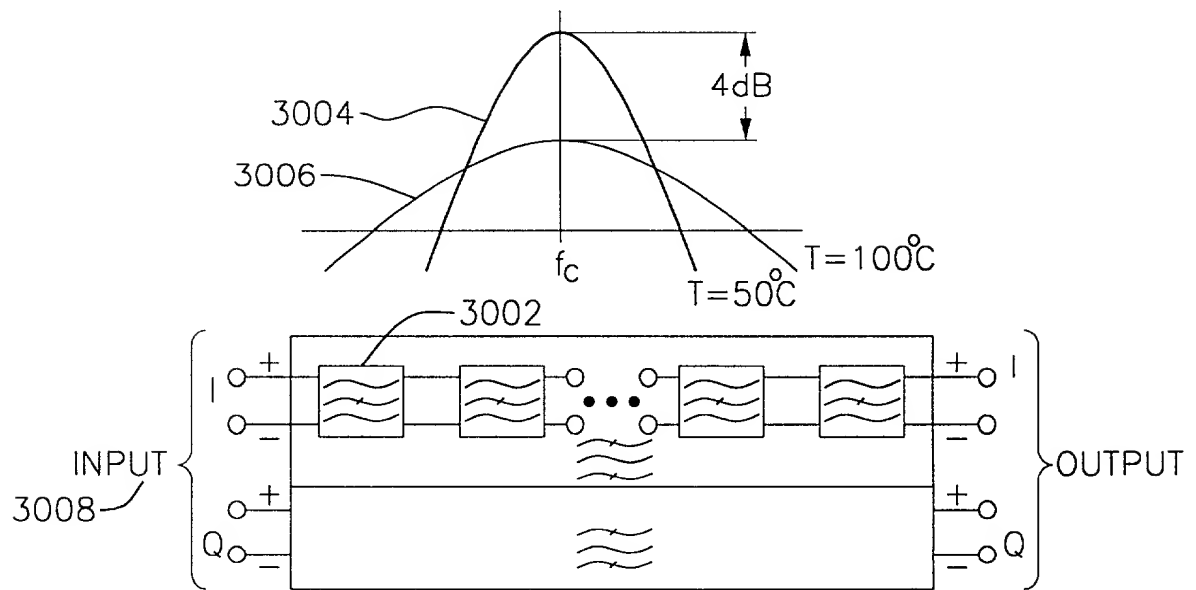


FIG. 31a

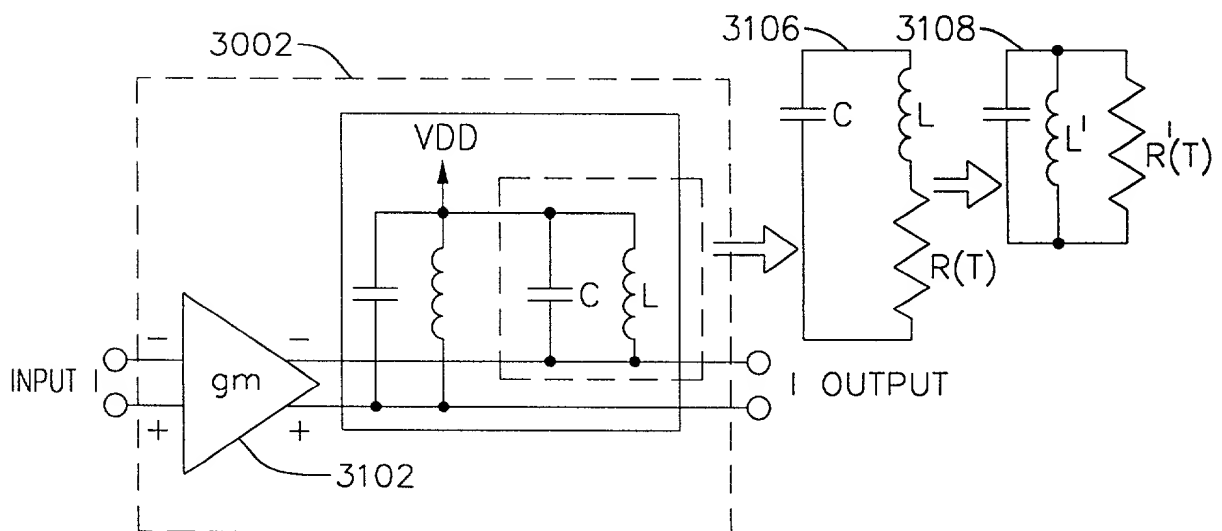


FIG. 31b

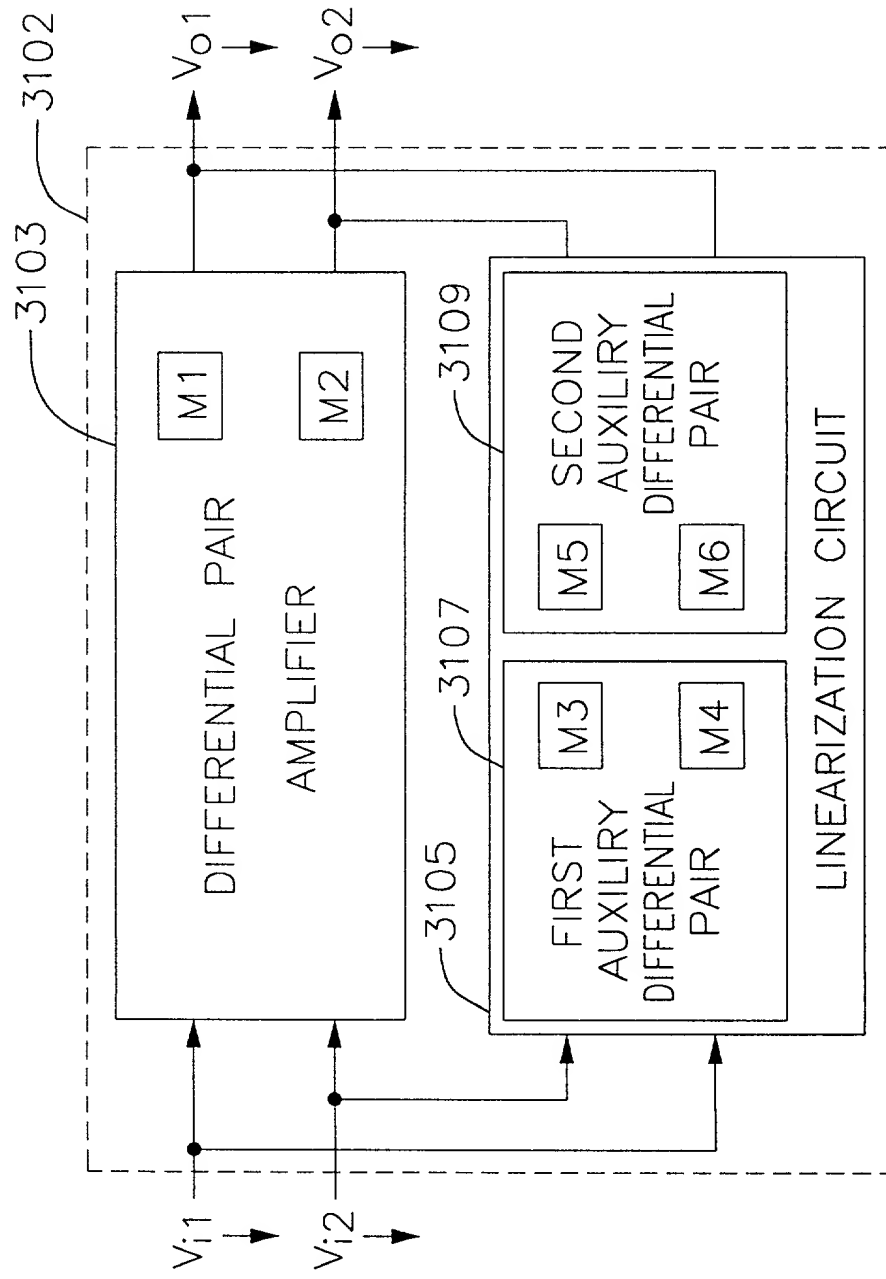


FIG. 31c

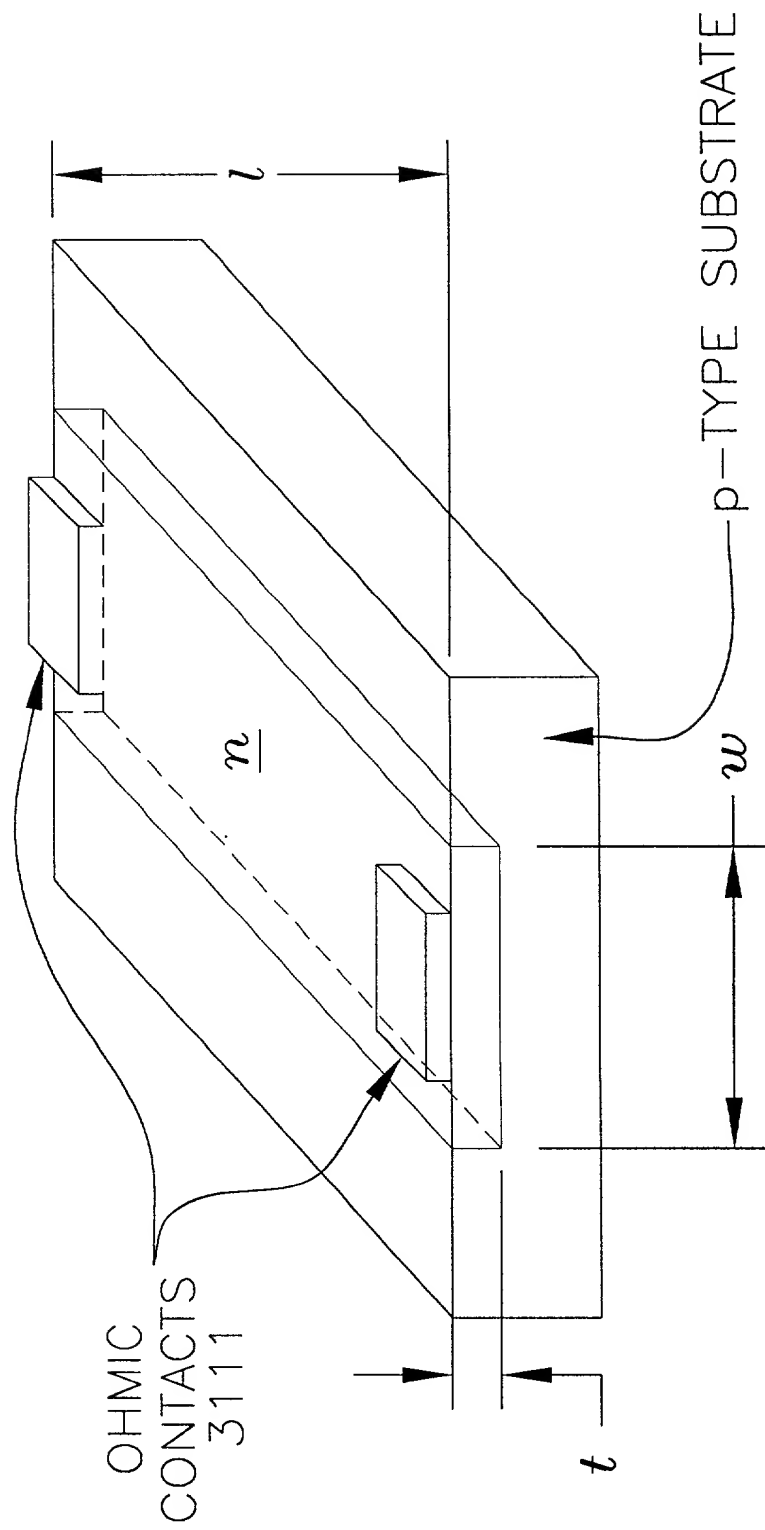


FIG. 31d

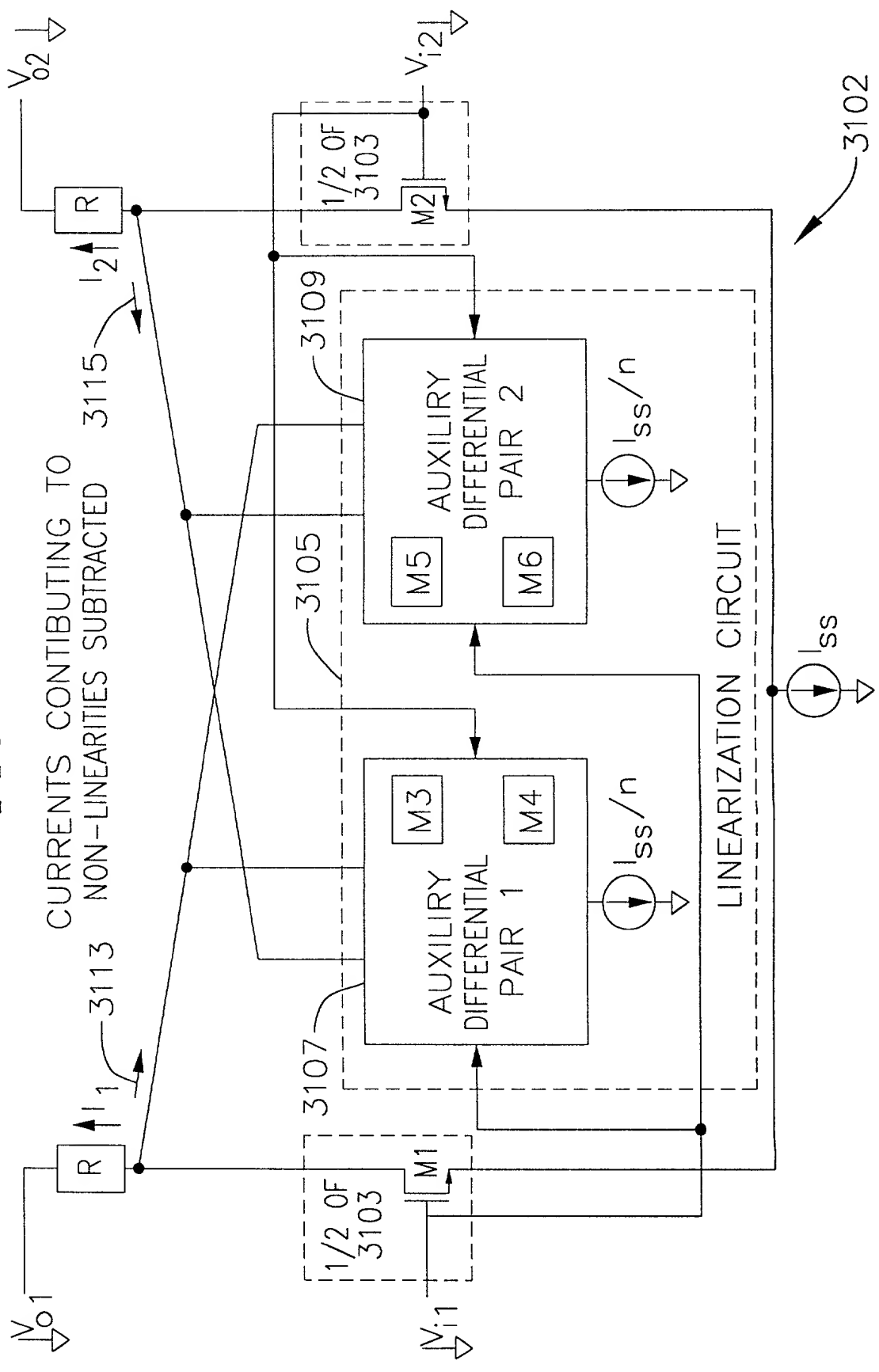


FIG. 31e

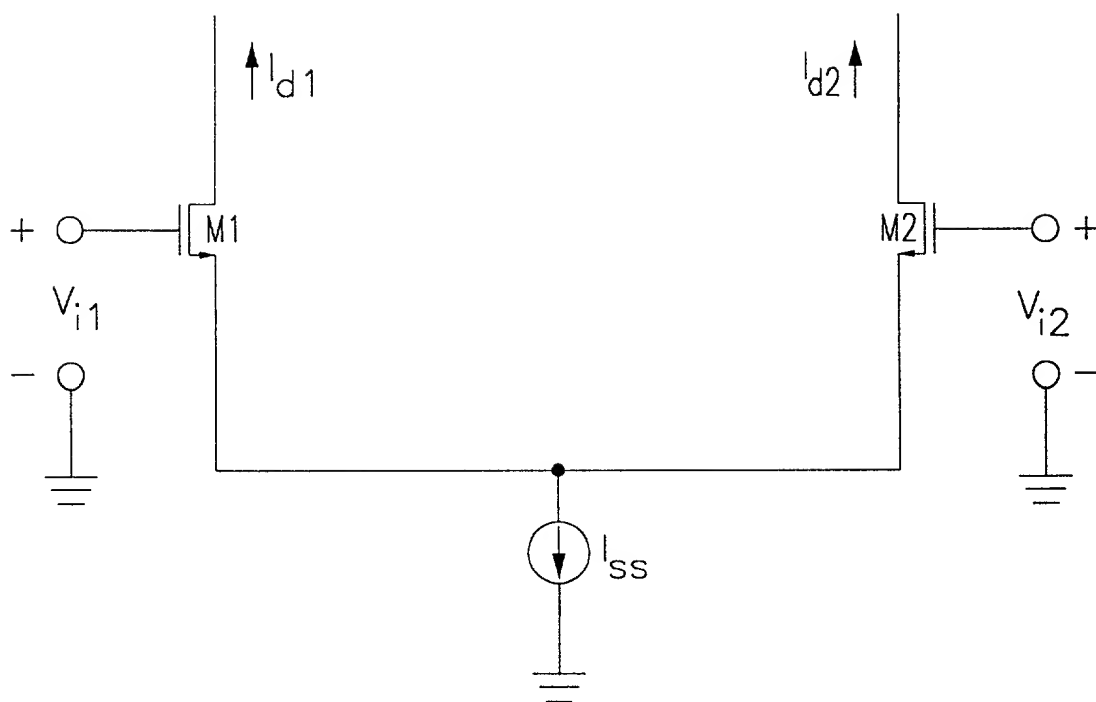


FIG. 31f

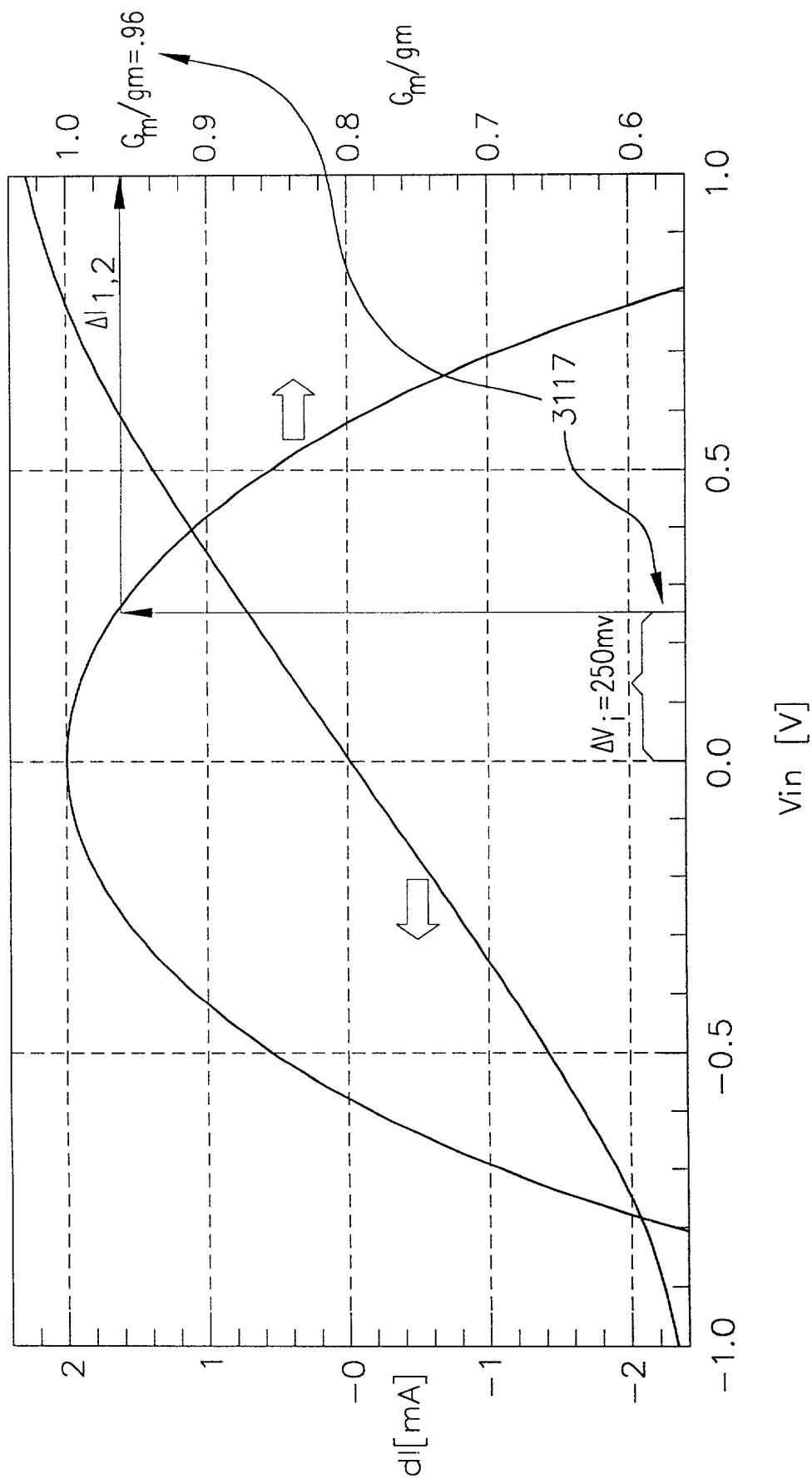


FIG. 31g

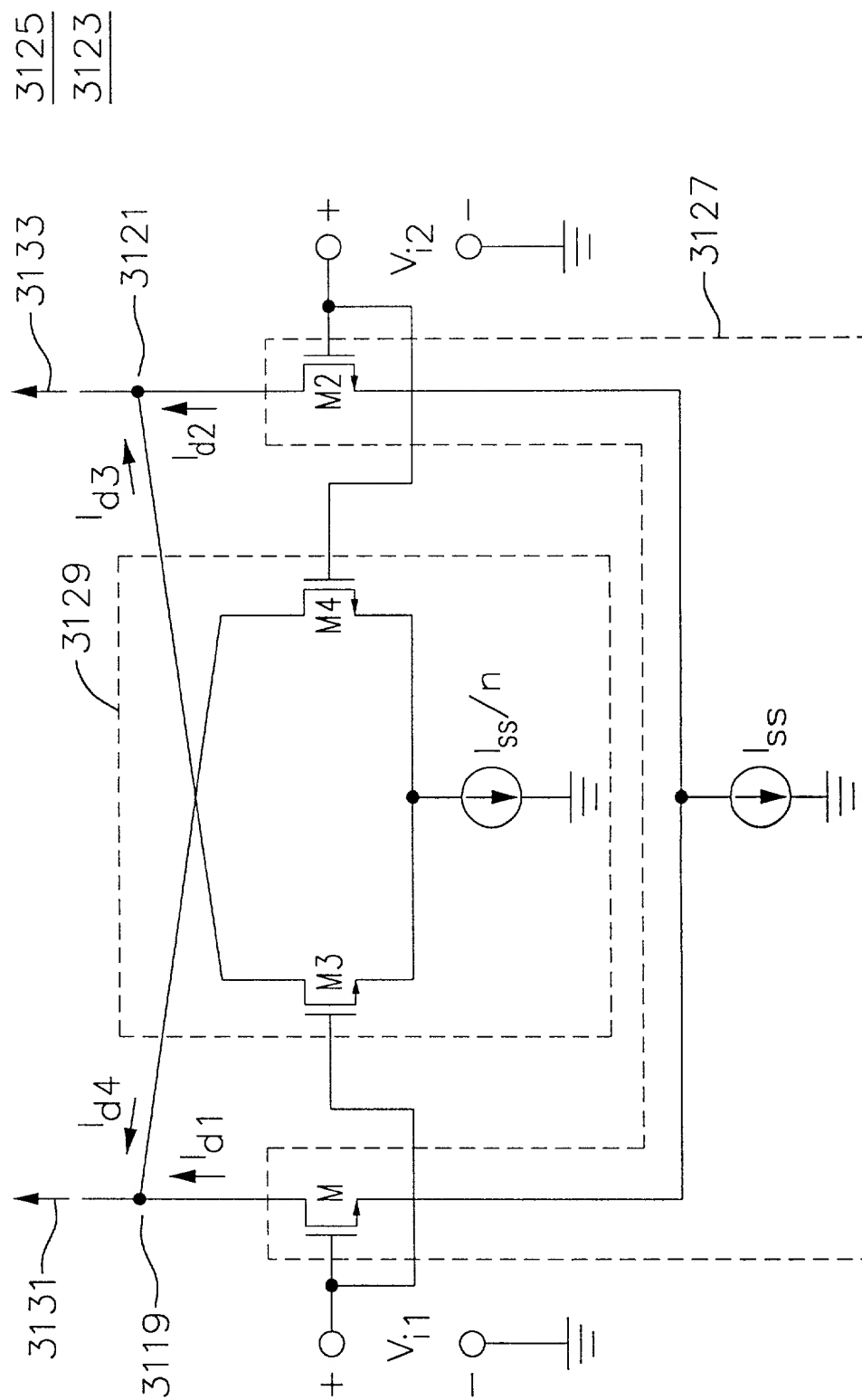


FIG. 31h

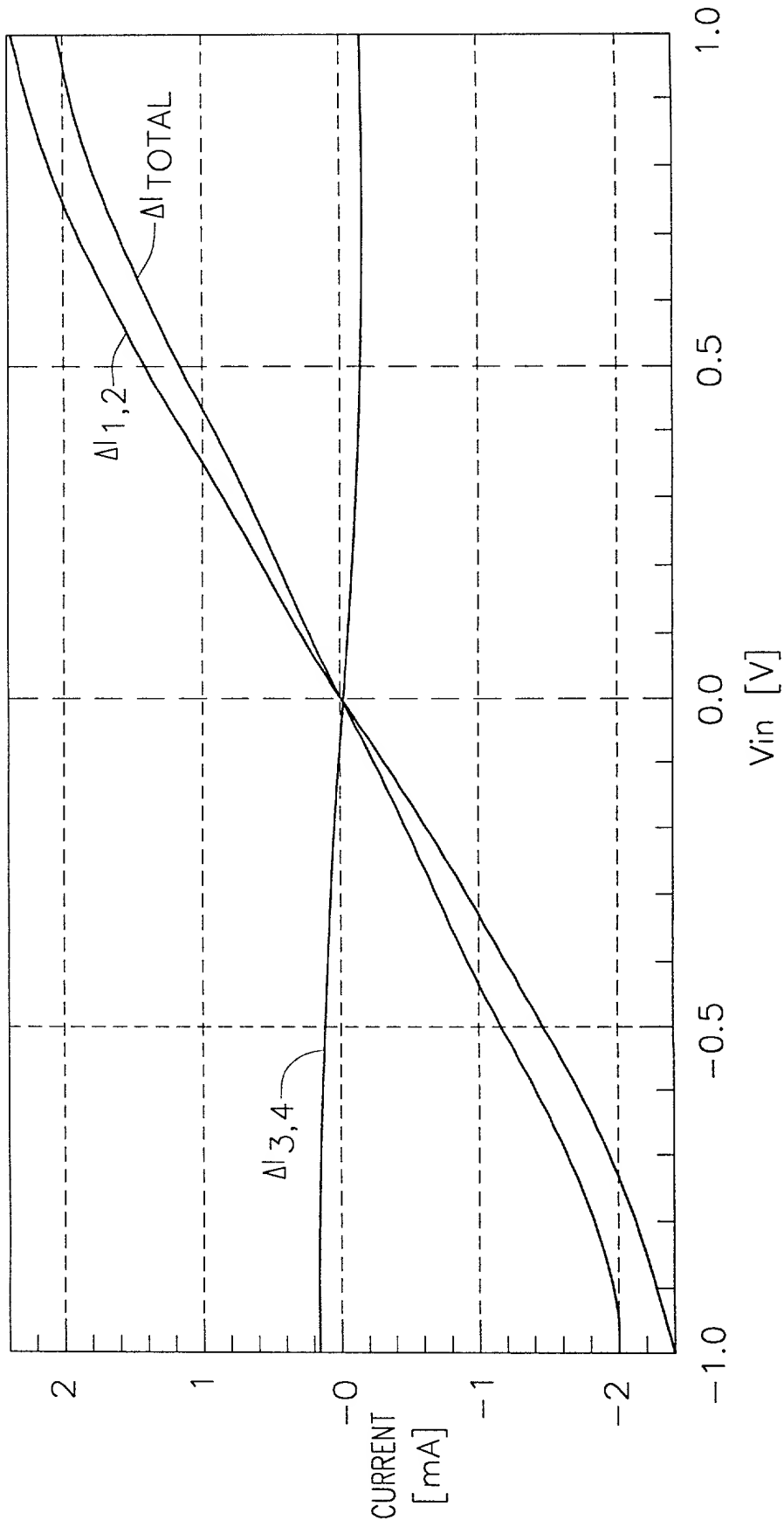


FIG. 31i

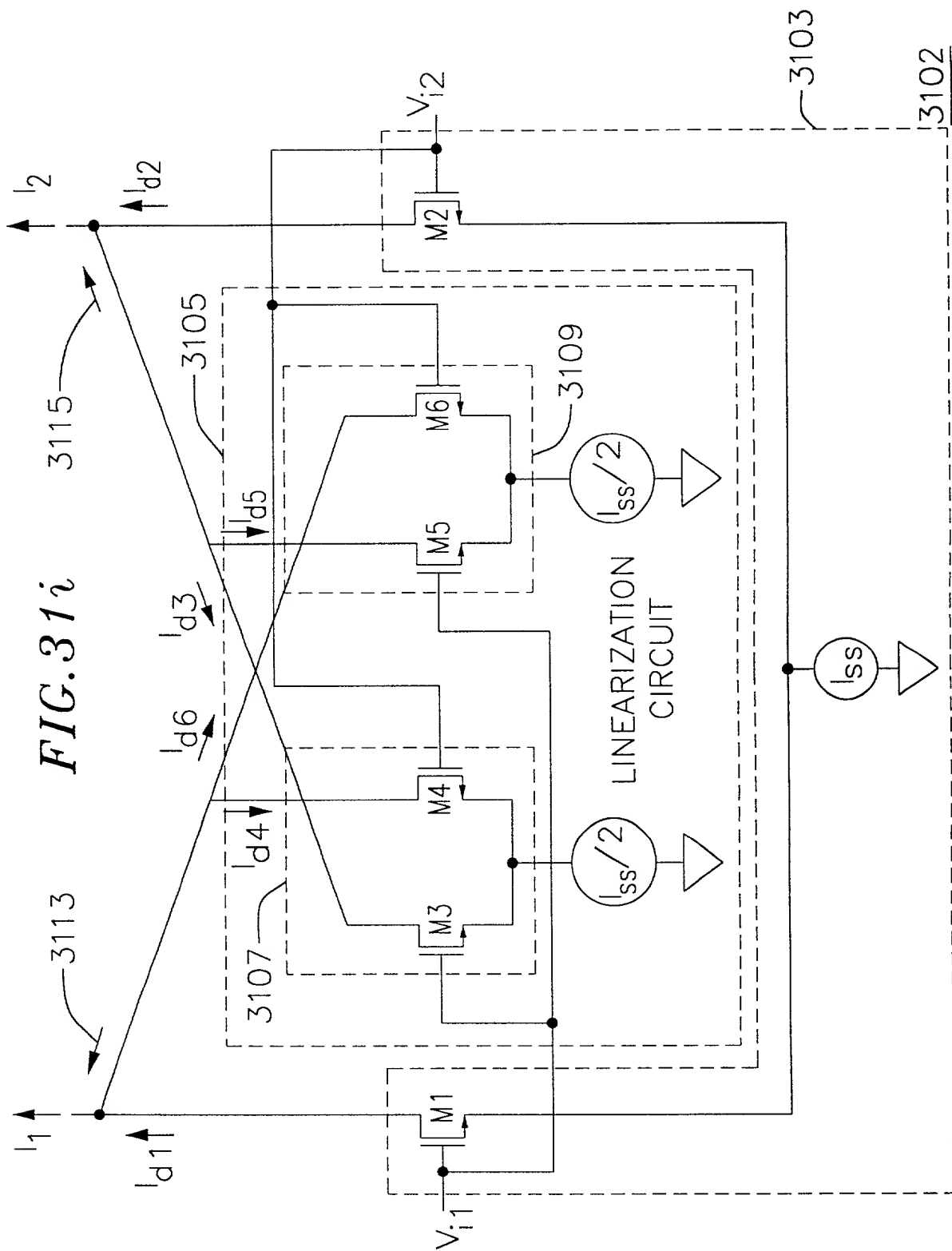


FIG. 31j

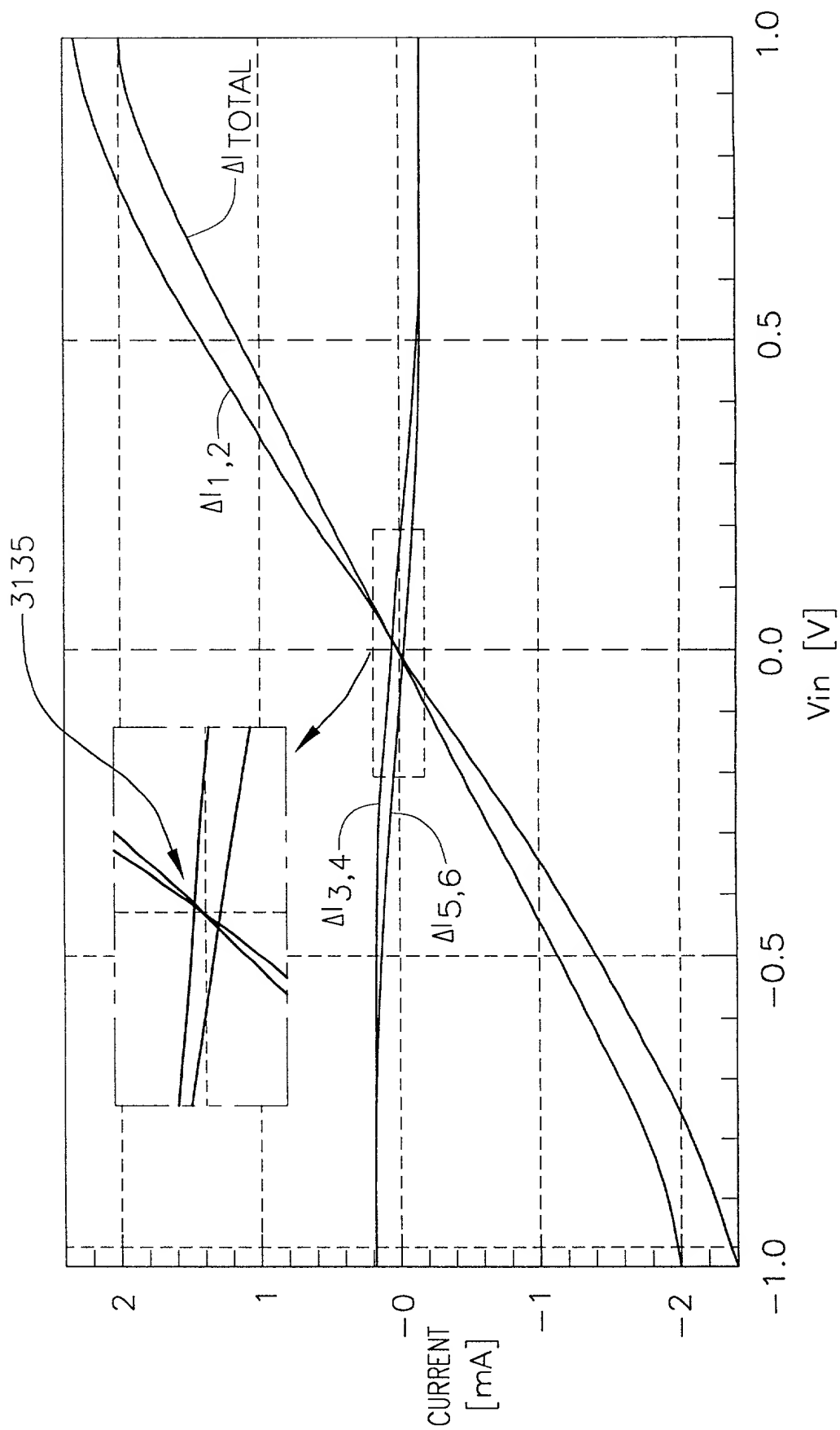


FIG. 31k

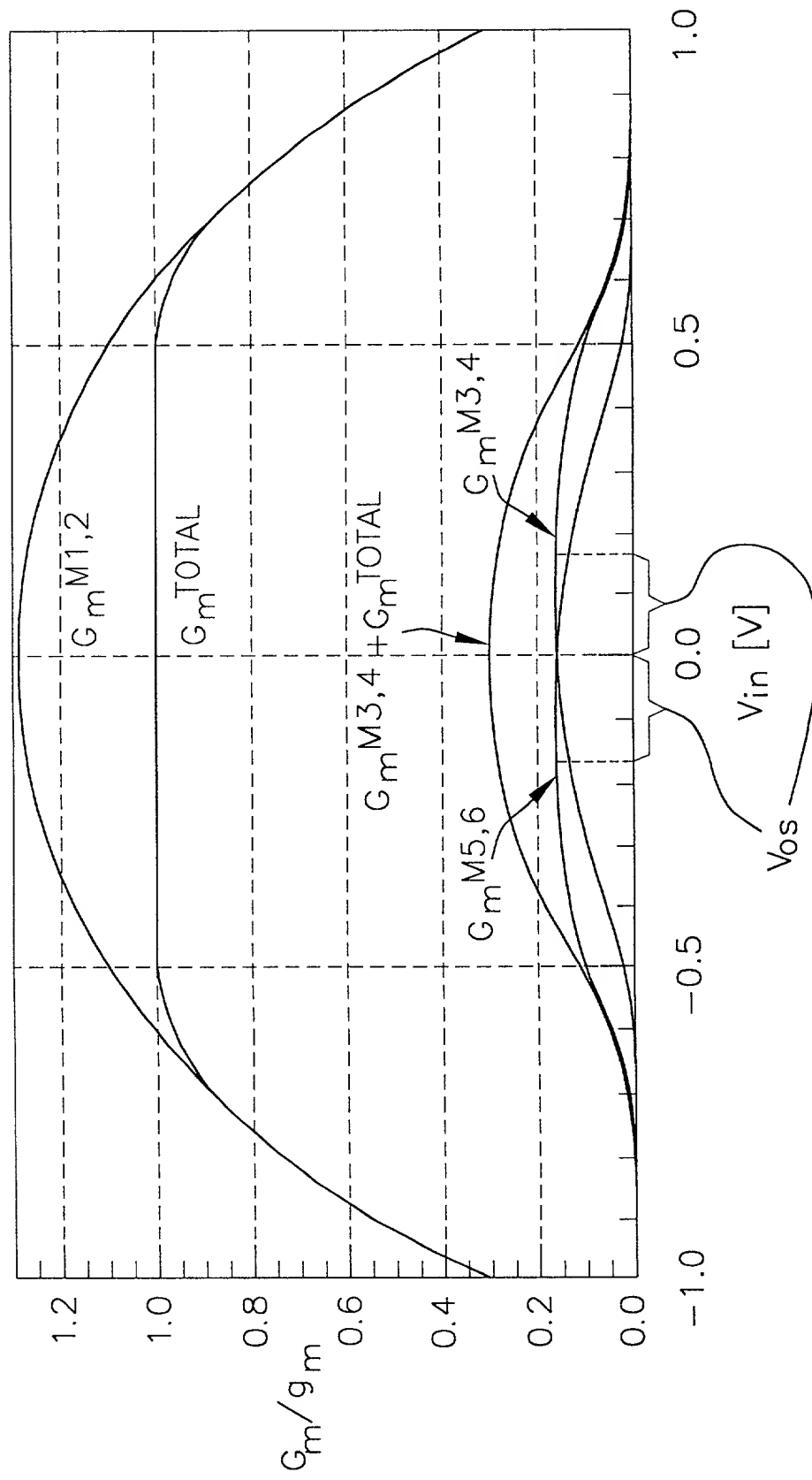


FIG. 31m

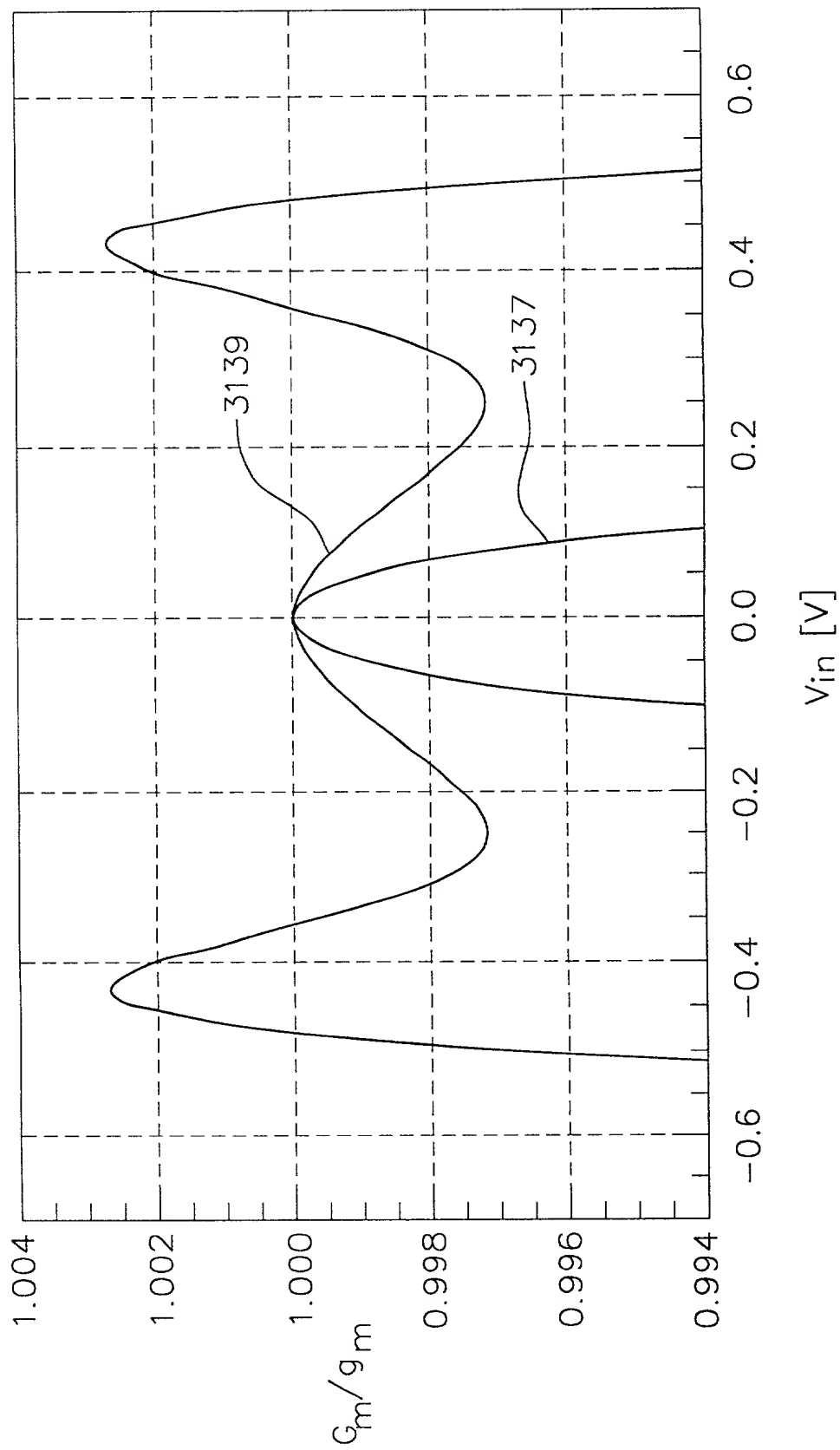


FIG. 34

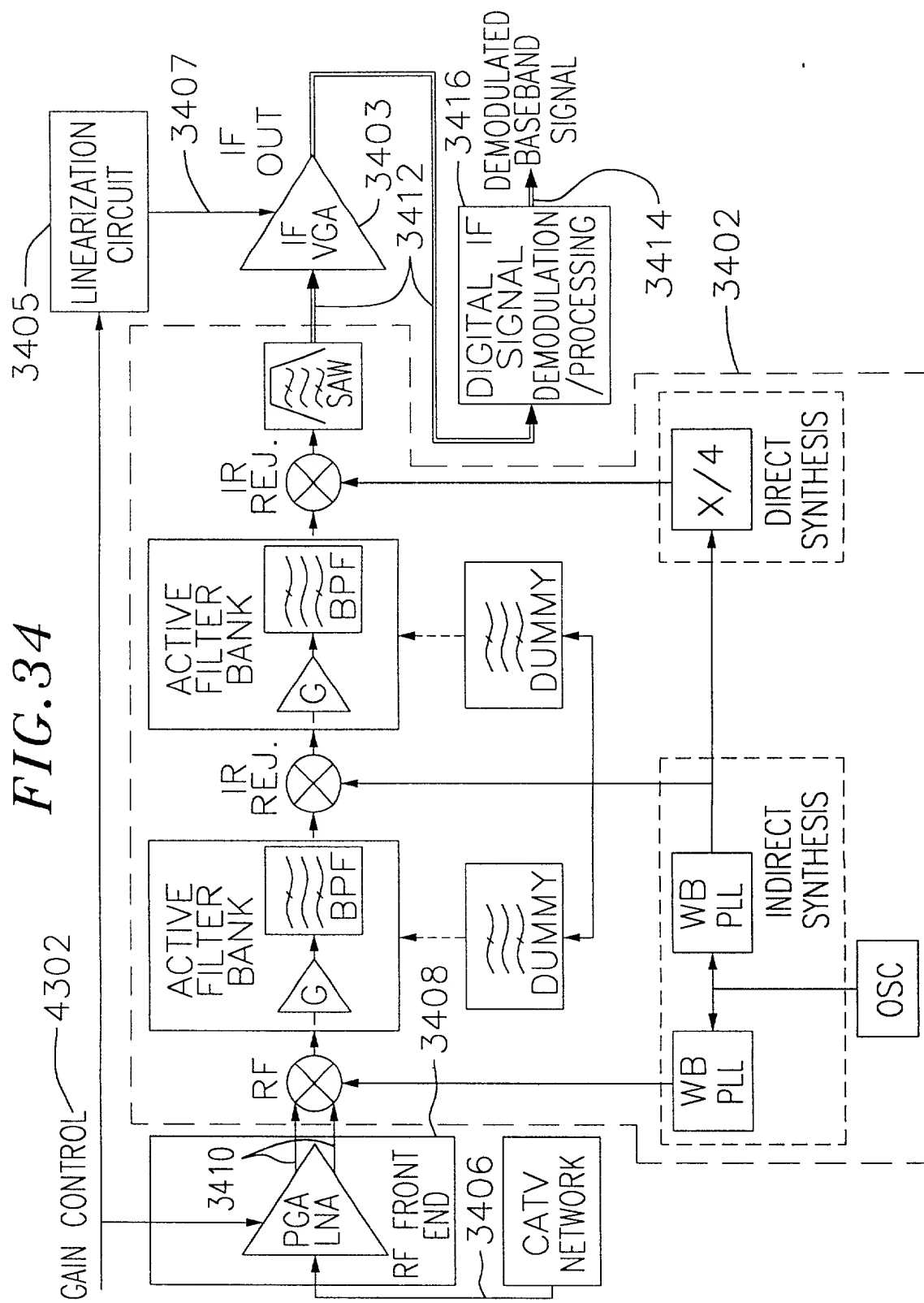


FIG. 35

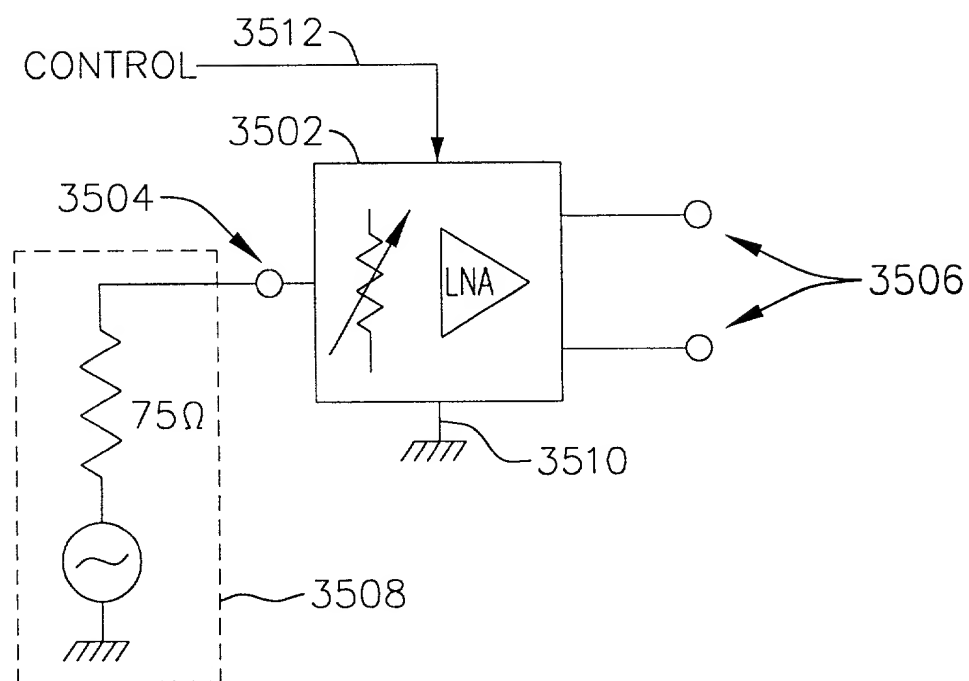


FIG. 36

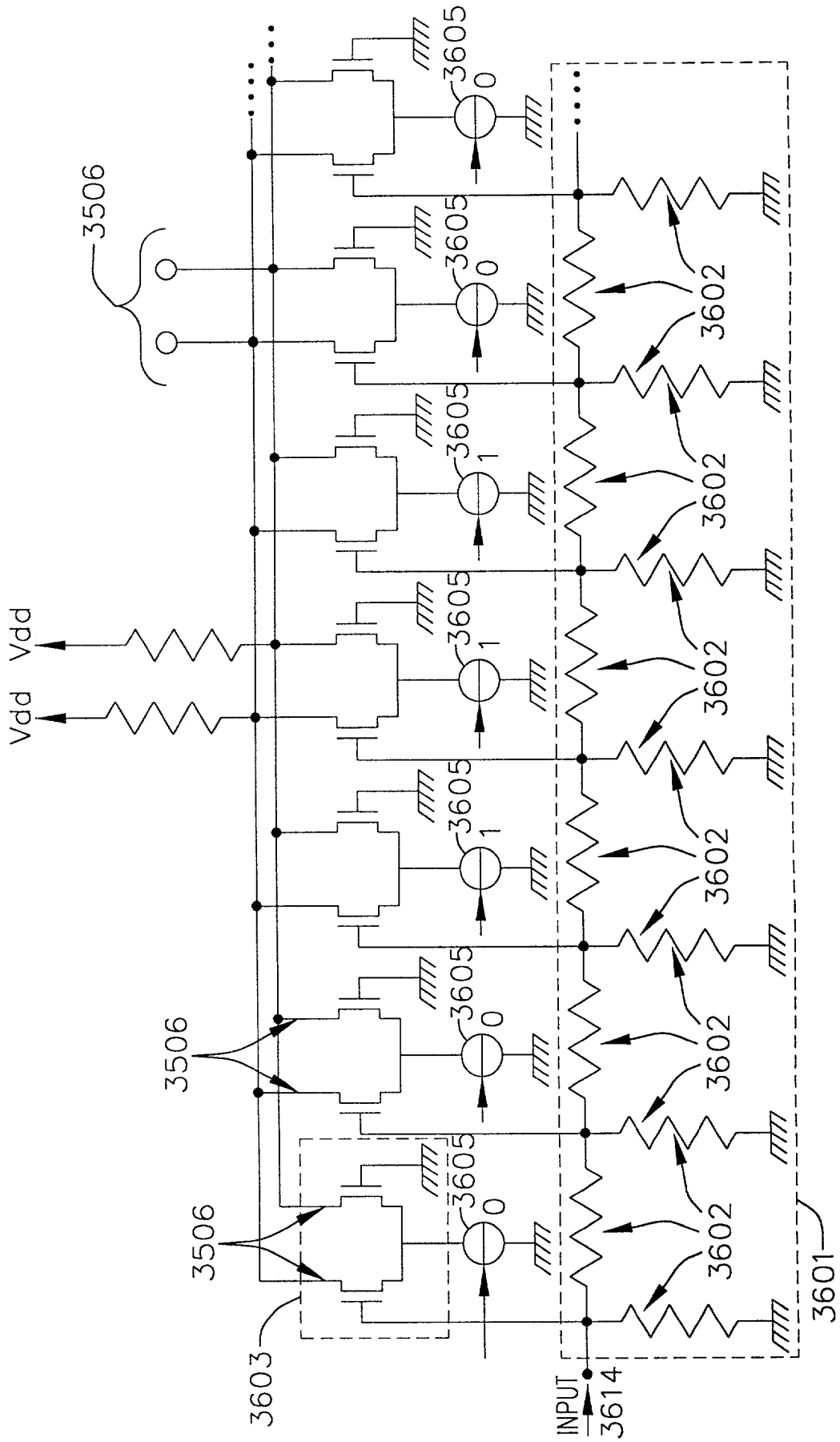


FIG. 37

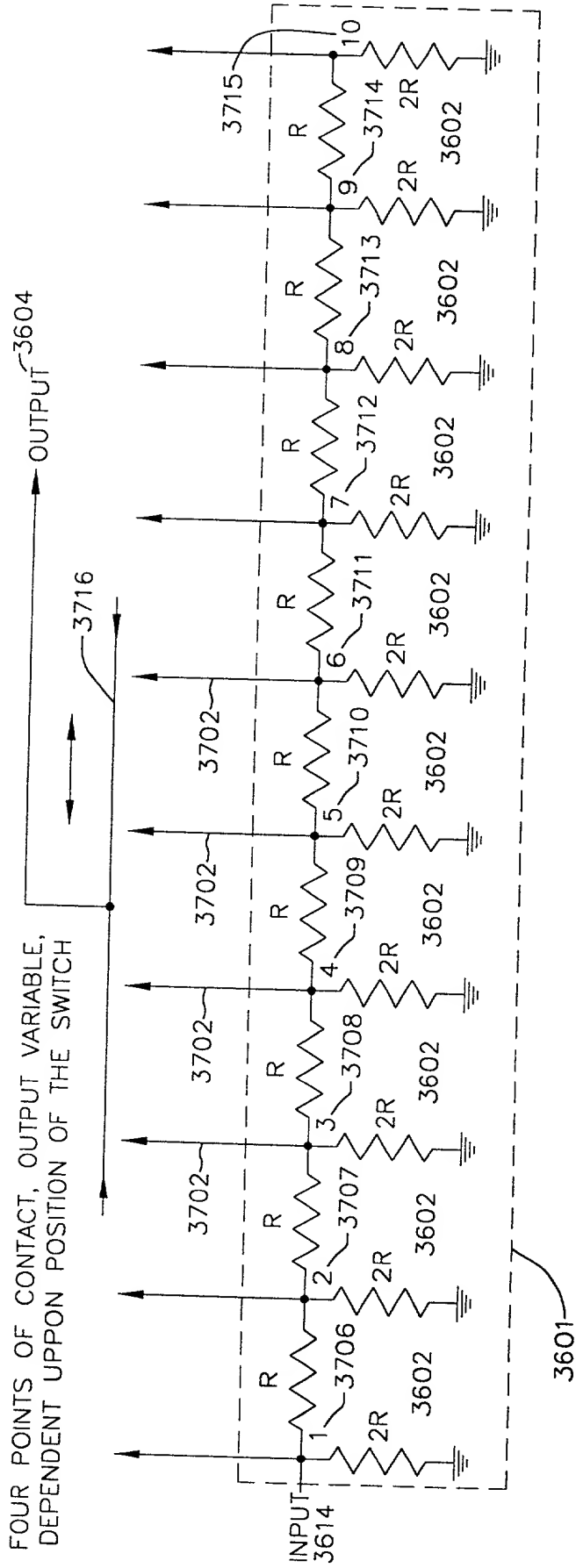


FIG. 38

PGA SETTINGS

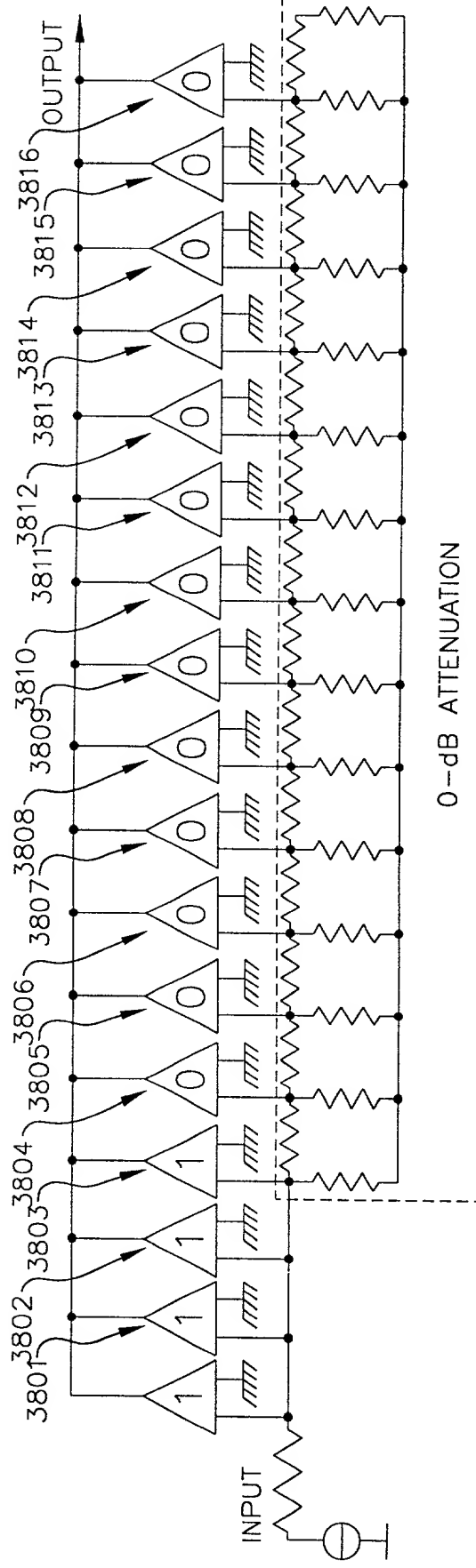


FIG. 39

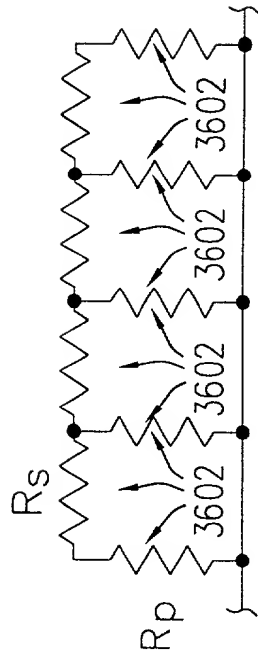


FIG. 40

PGA ARCHITECTURE

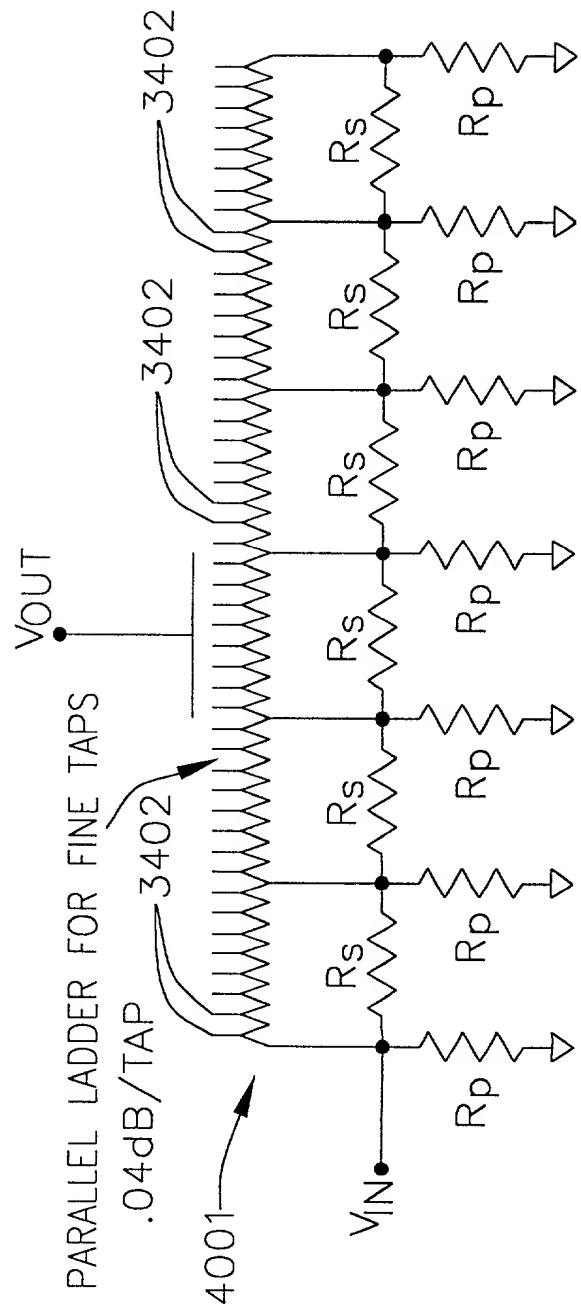


FIG. 41

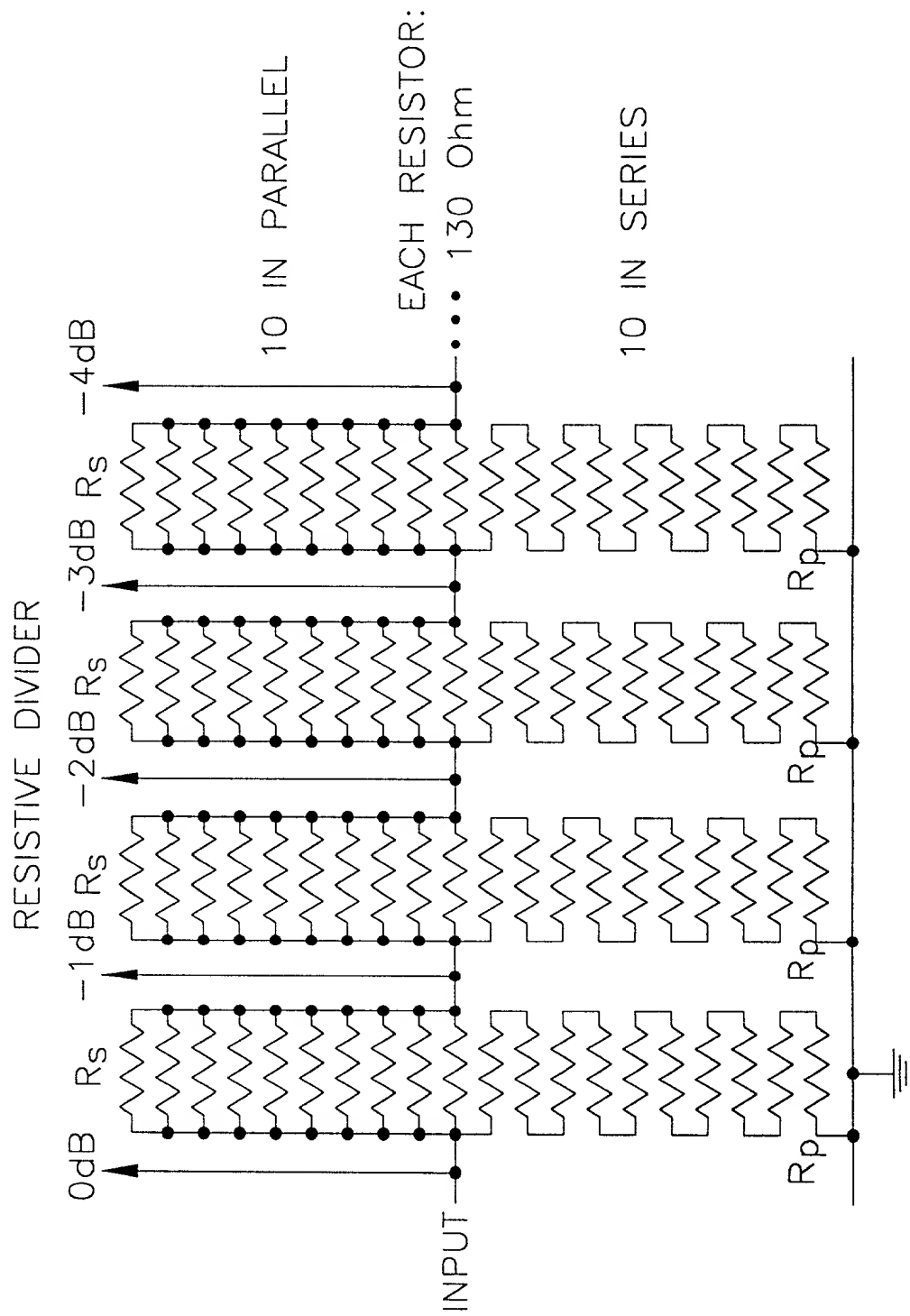


FIG. 42

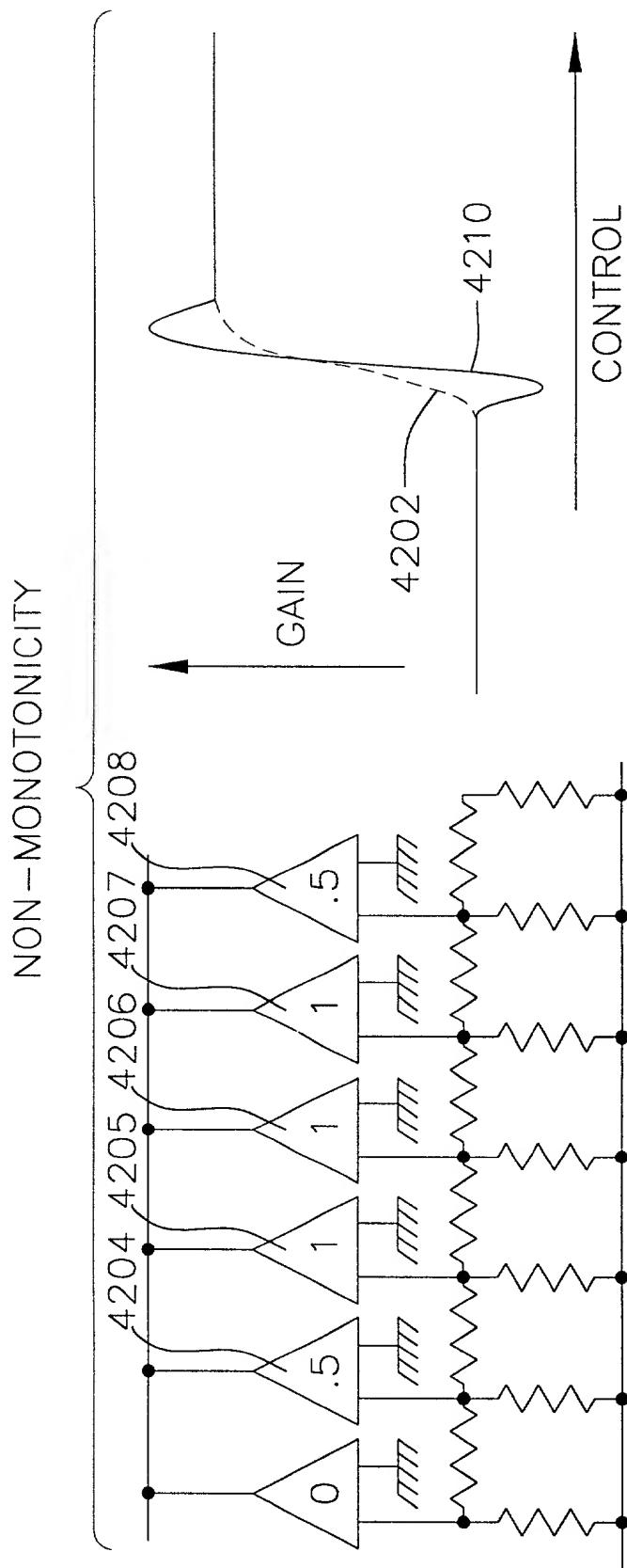


FIG. 43

CLAMPING CONTROL RANGE

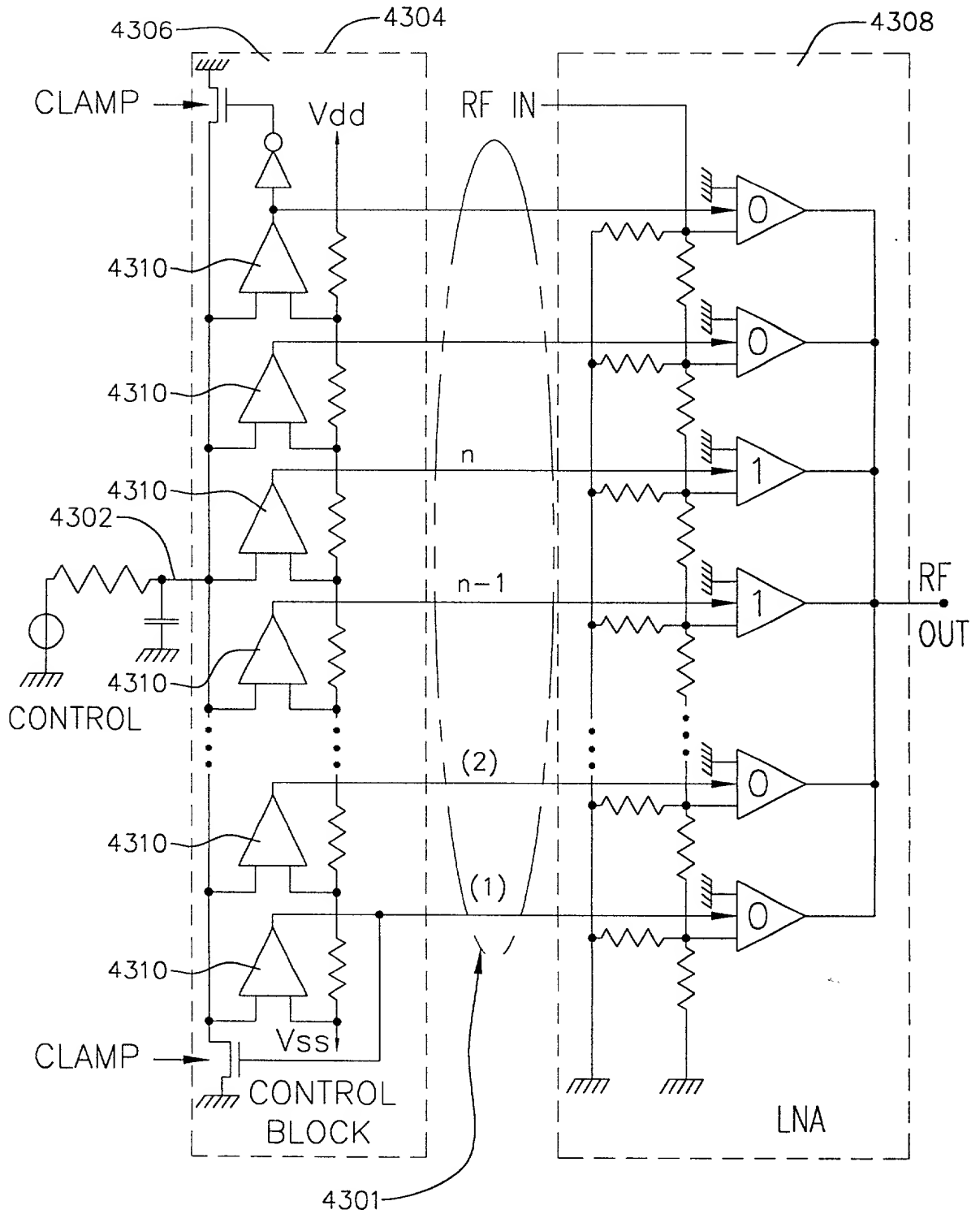


FIG. 45a

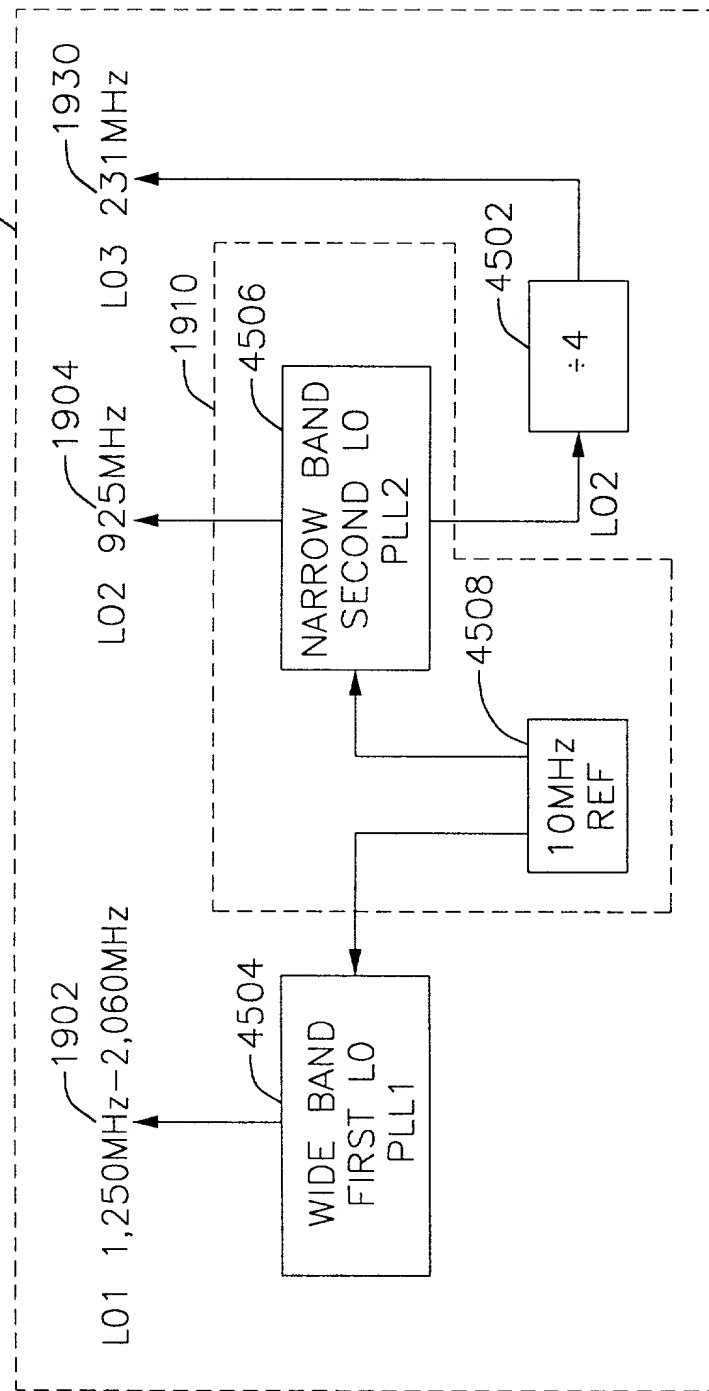


FIG. 455b

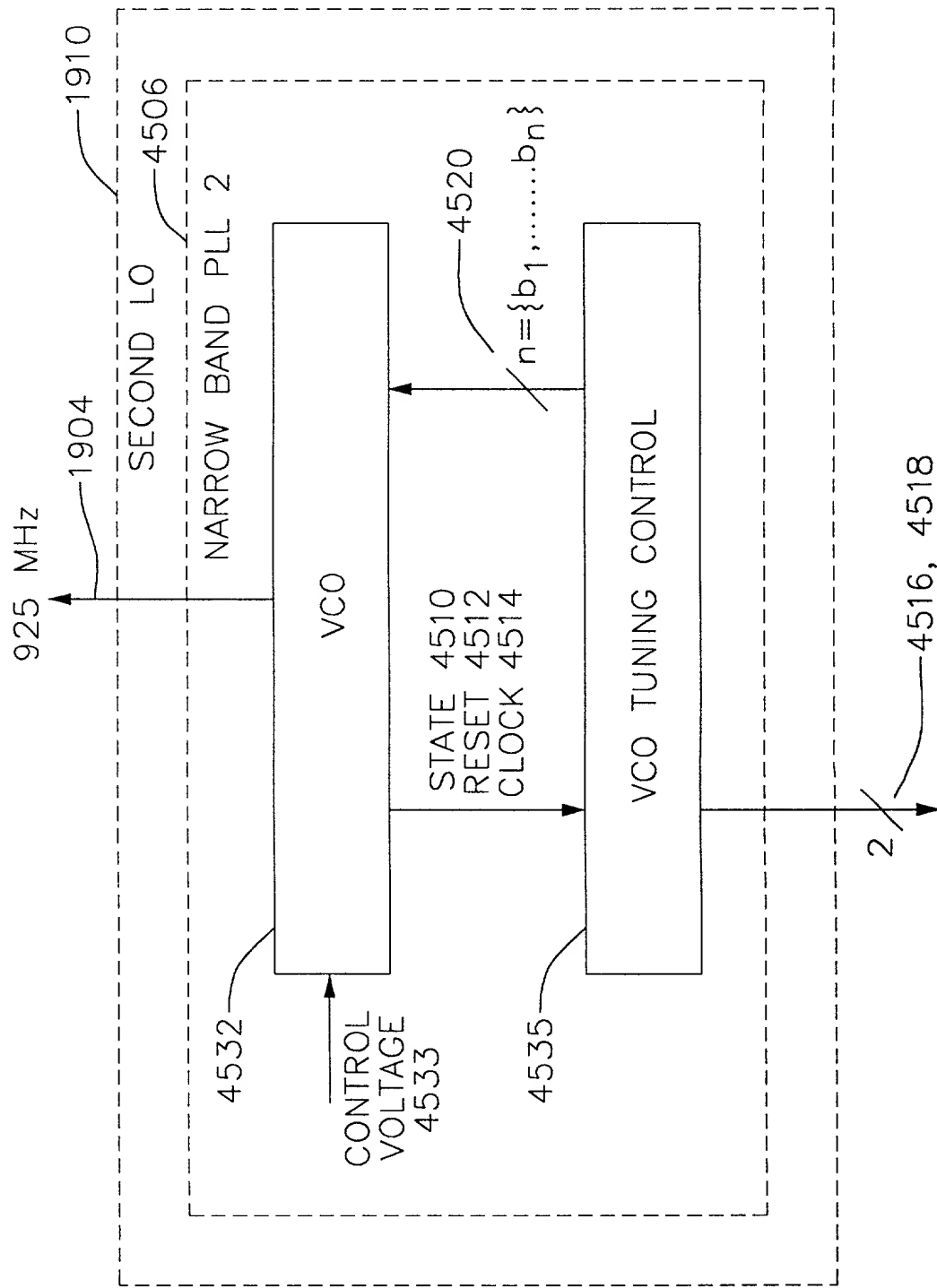


FIG. 450c

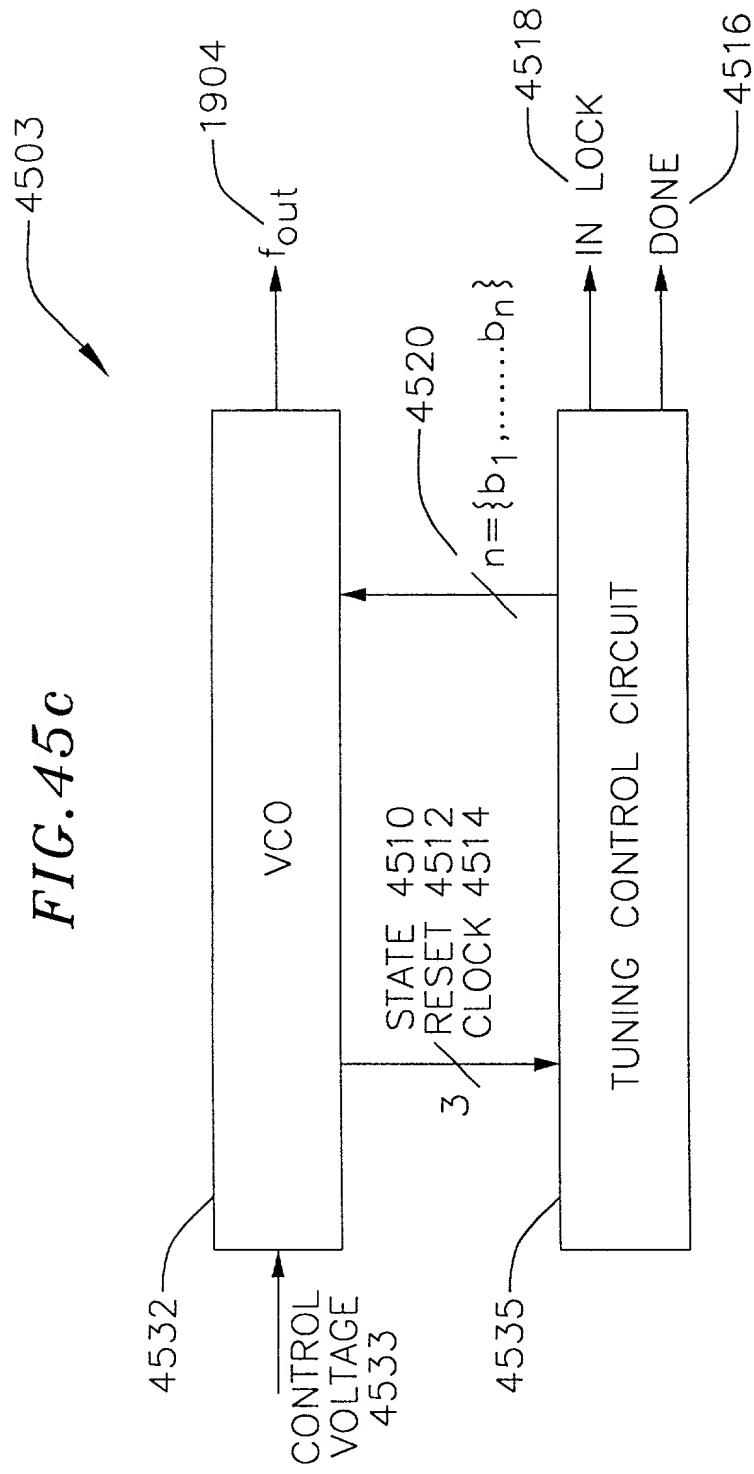


FIG. 45d

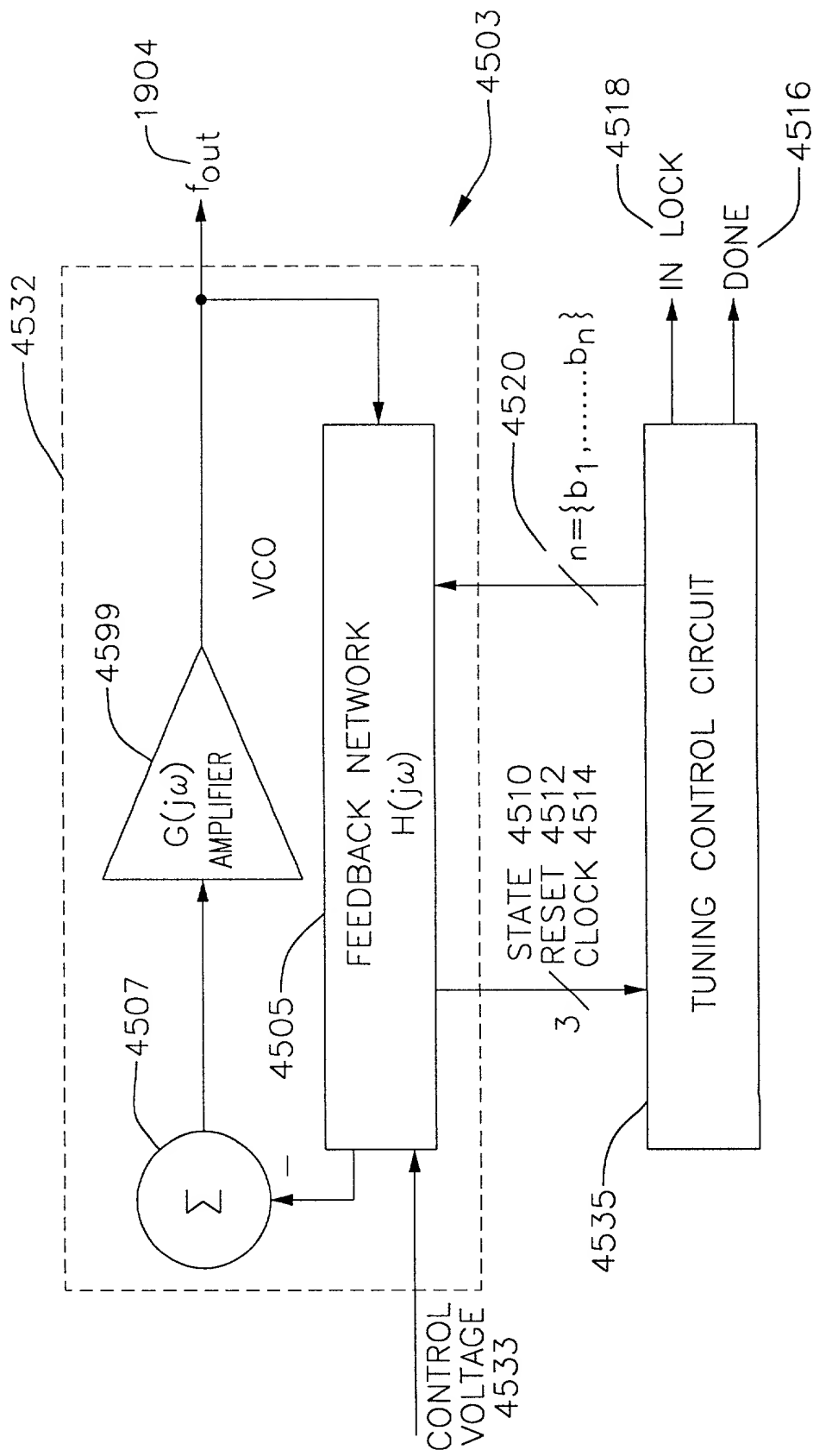


FIG. 45e

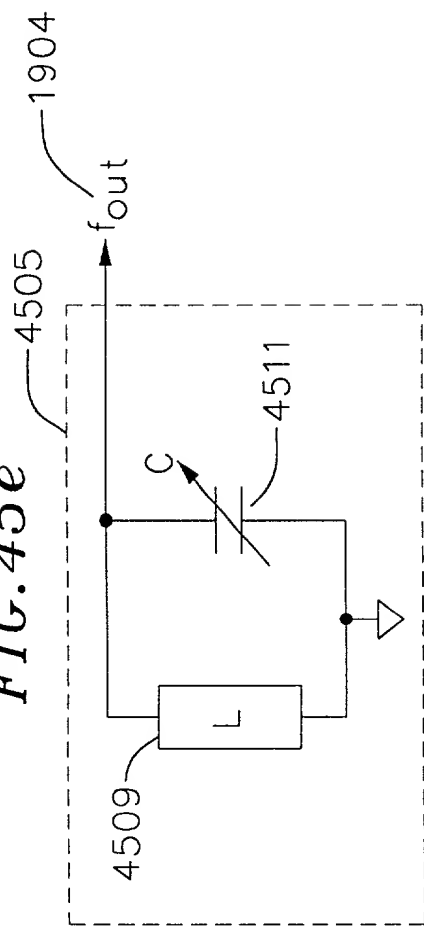


FIG. 45f

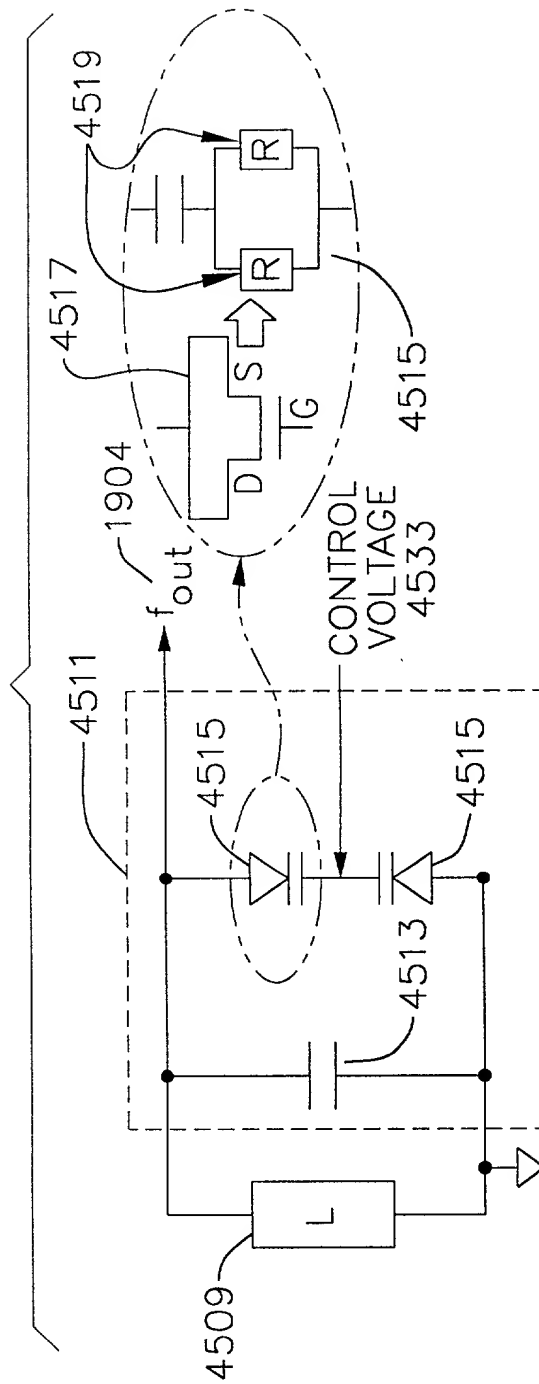


FIG. 45g

CAPACITANCE VS CONTROL VOLTAGE

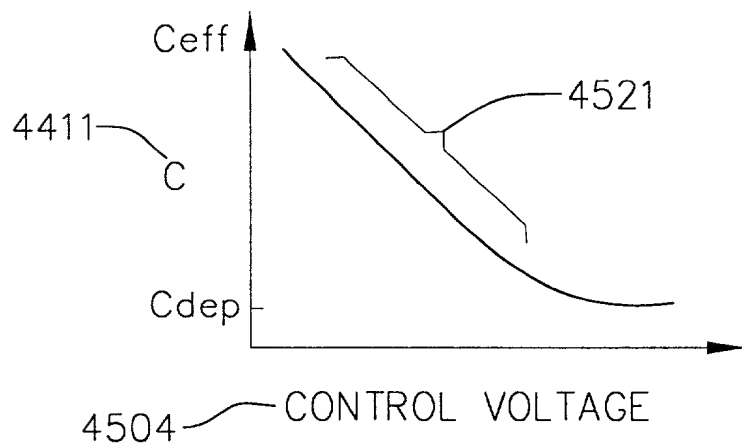


FIG. 45h

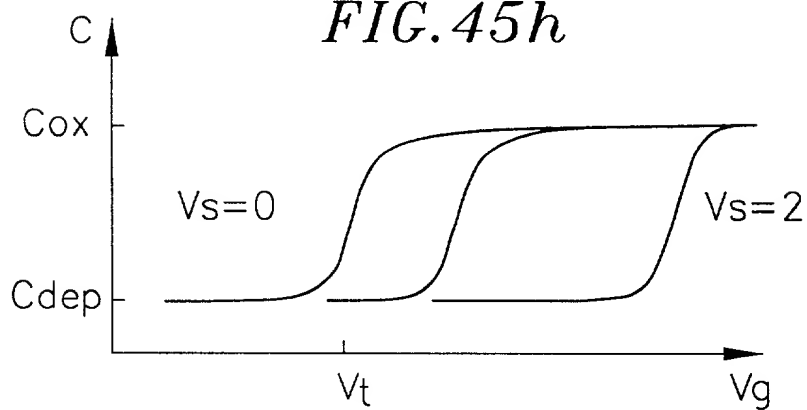


FIG. 45j

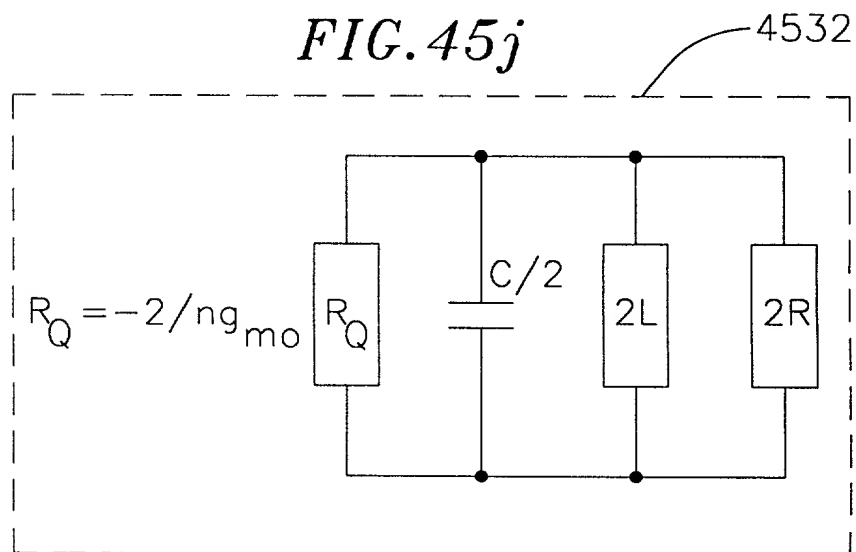


FIG. 45i

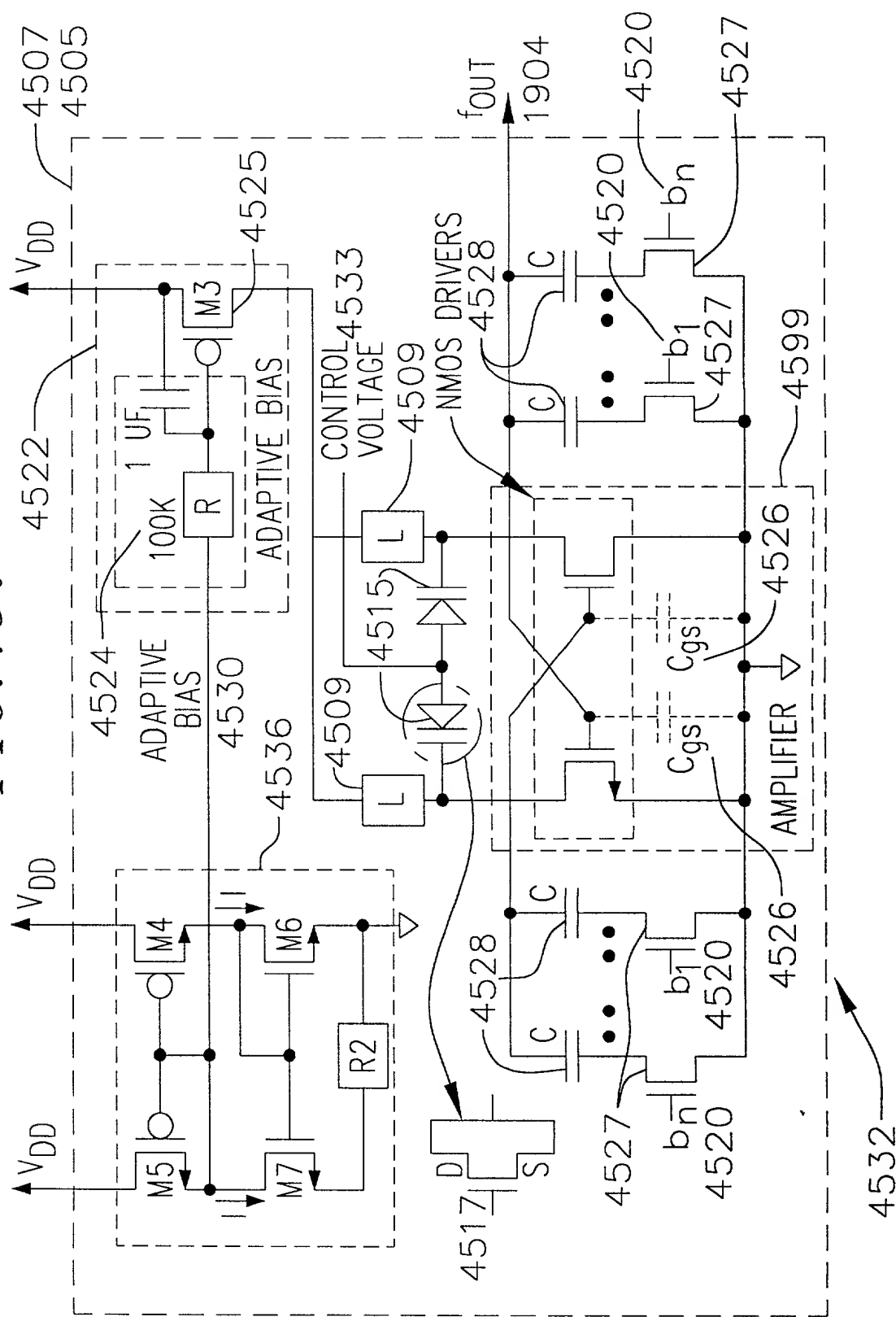


FIG. 45k

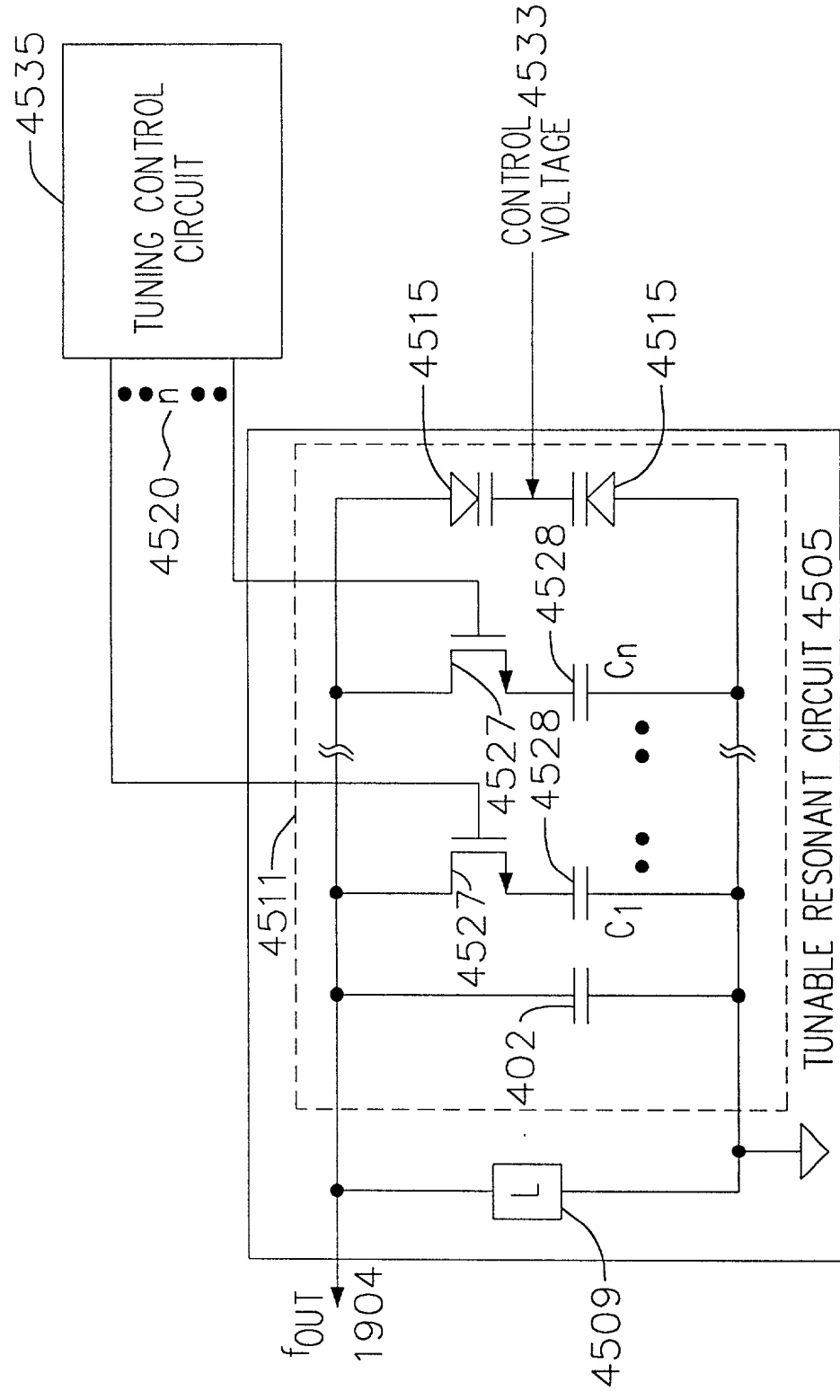


FIG. 46b

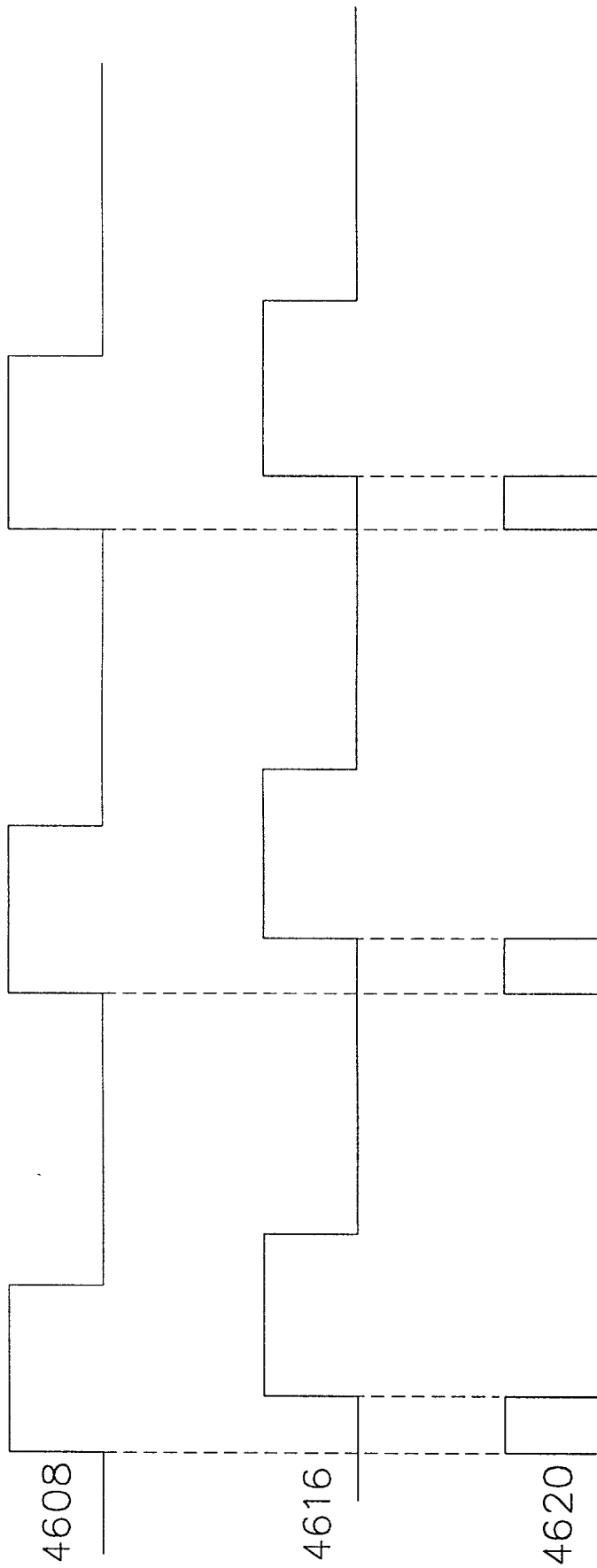


FIG. 47a

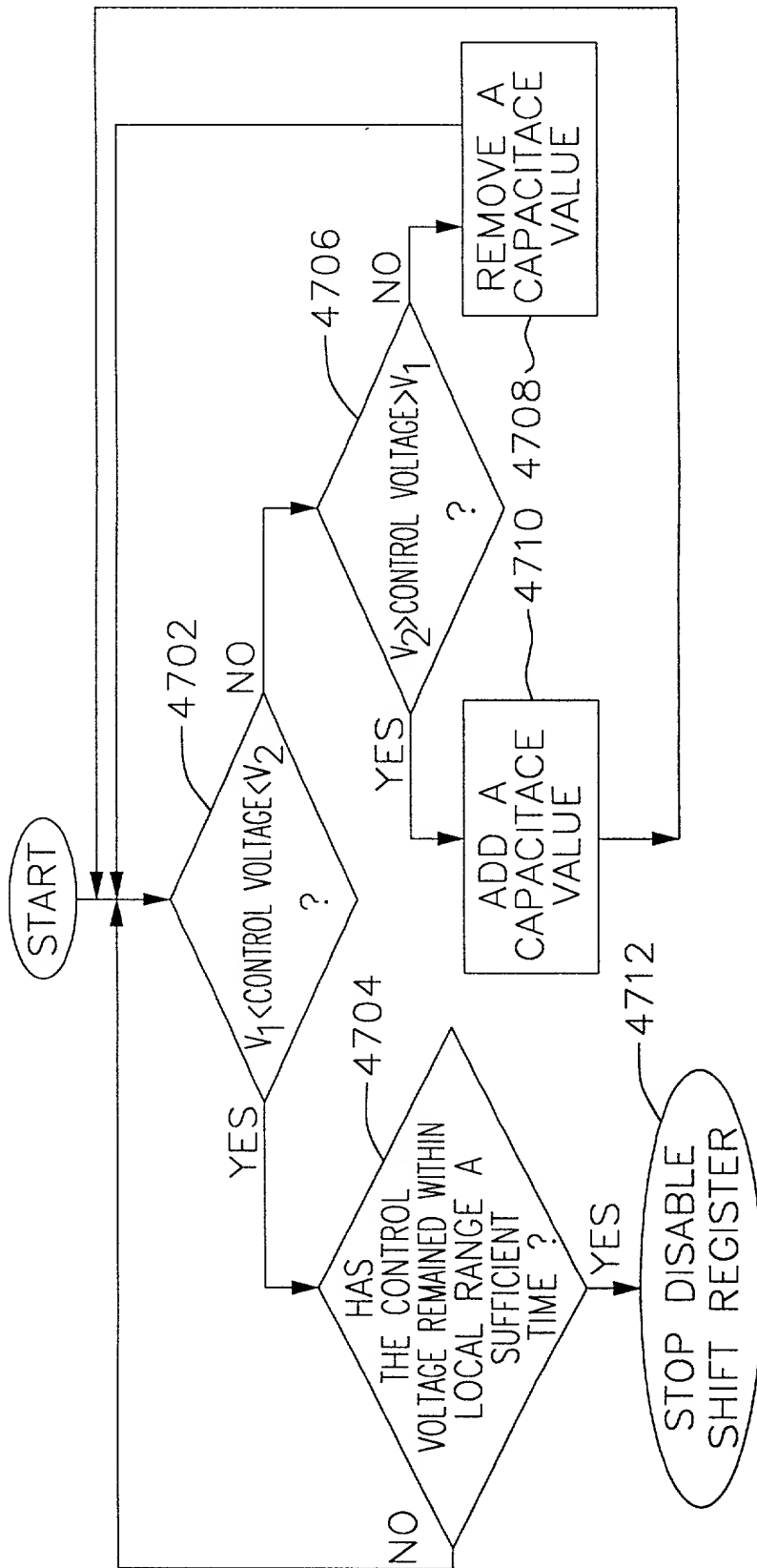
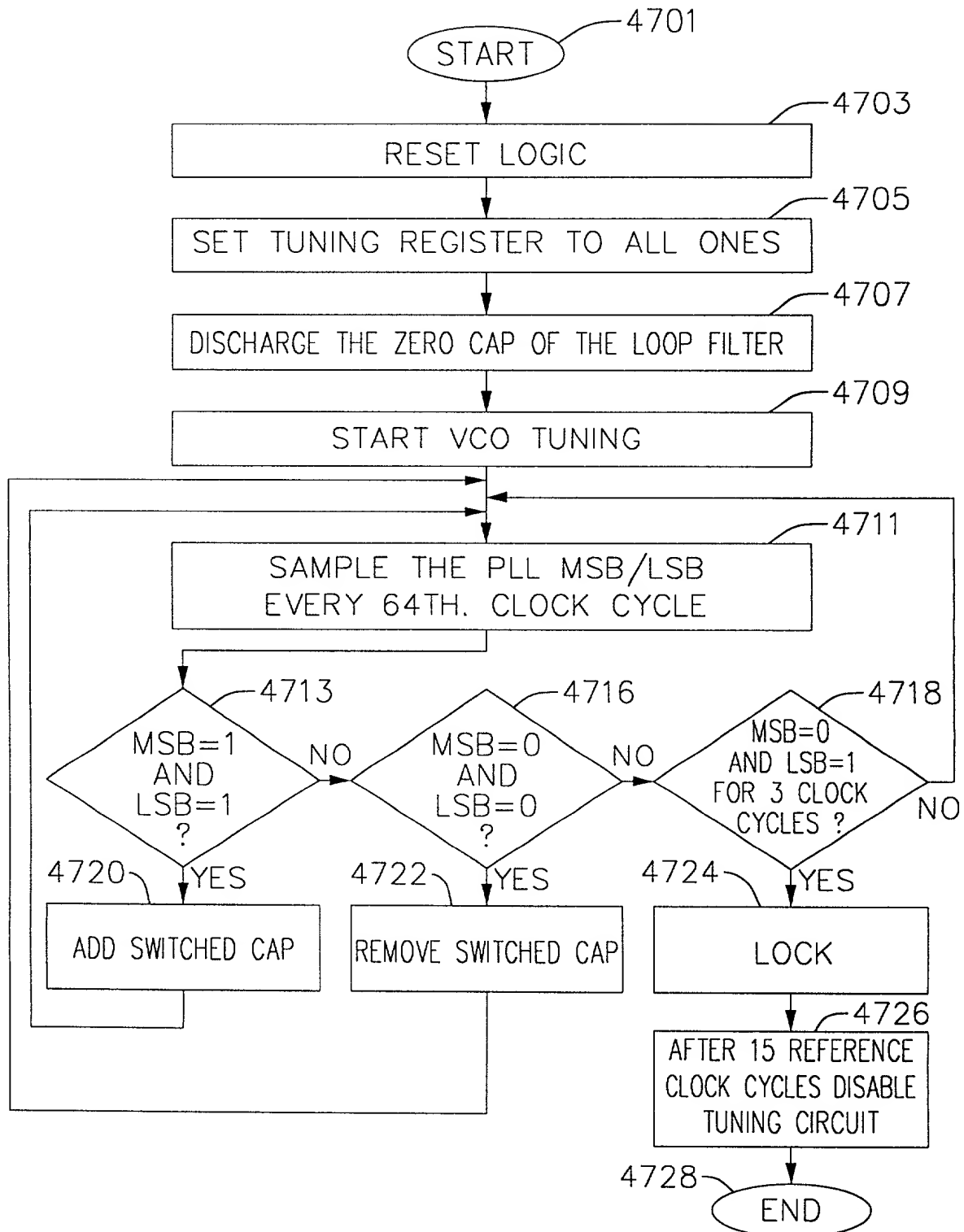


FIG. 47b



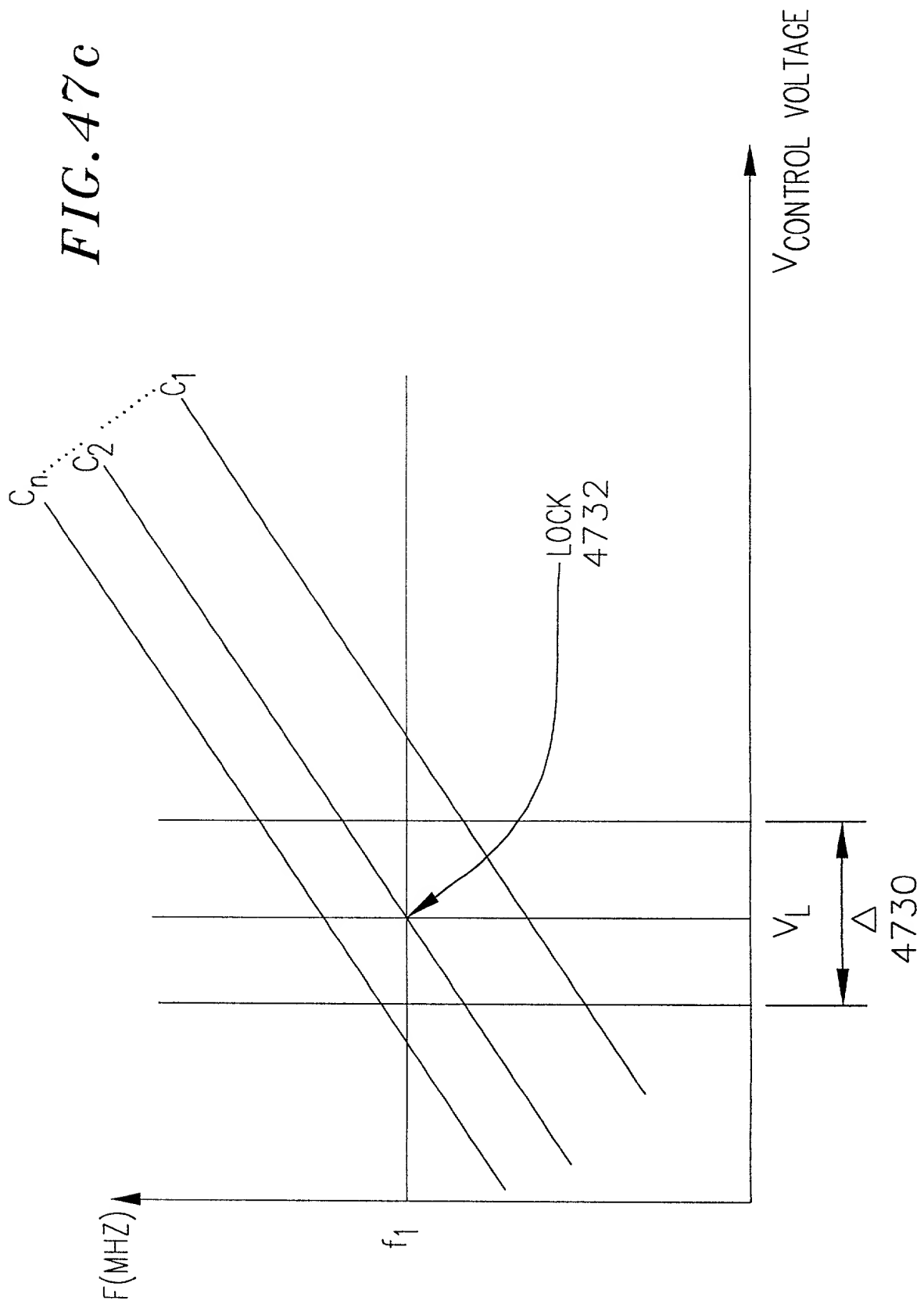


FIG. 47d

REPRESENTATIVE K_{VCO} CURVES

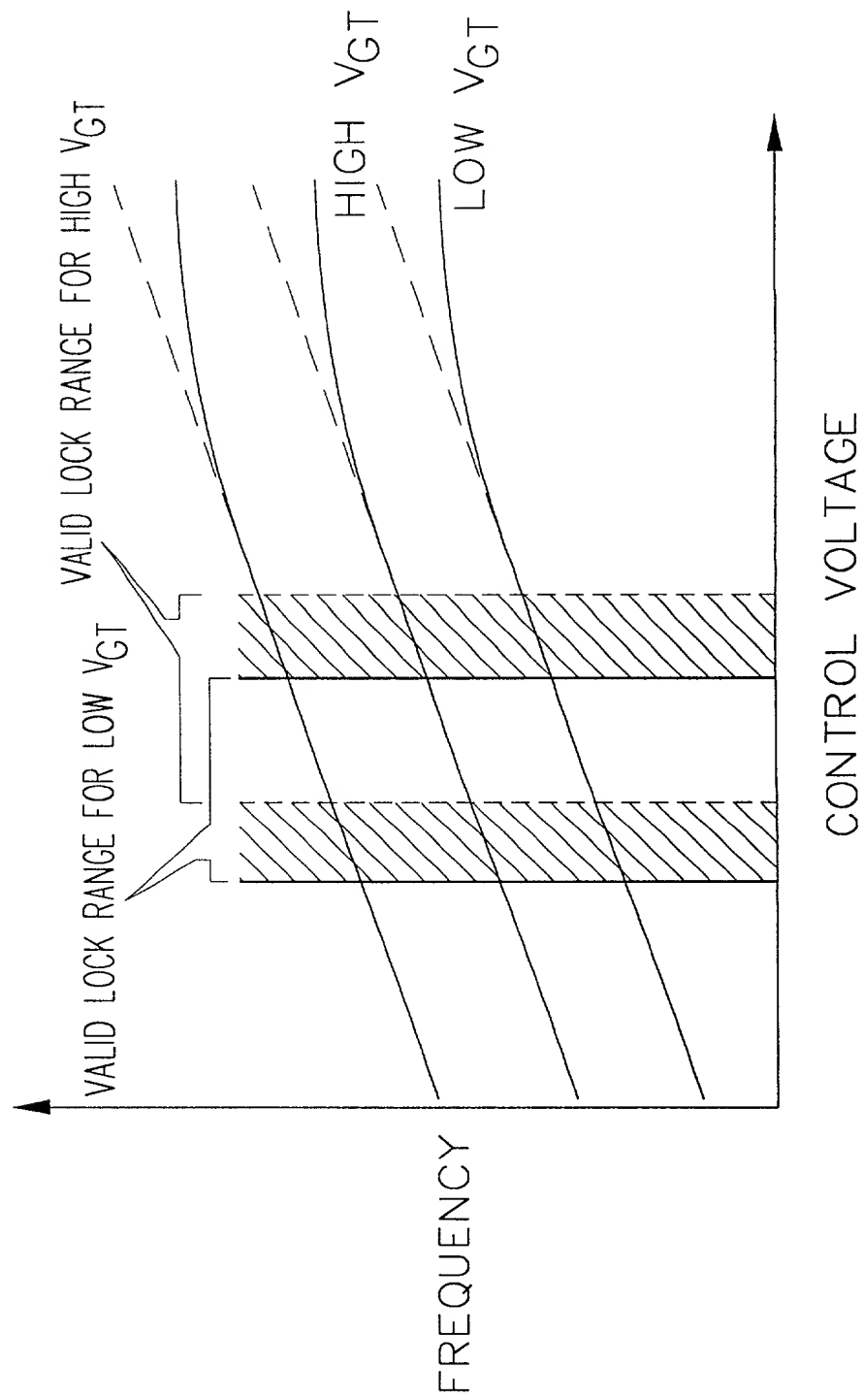


FIG. 48

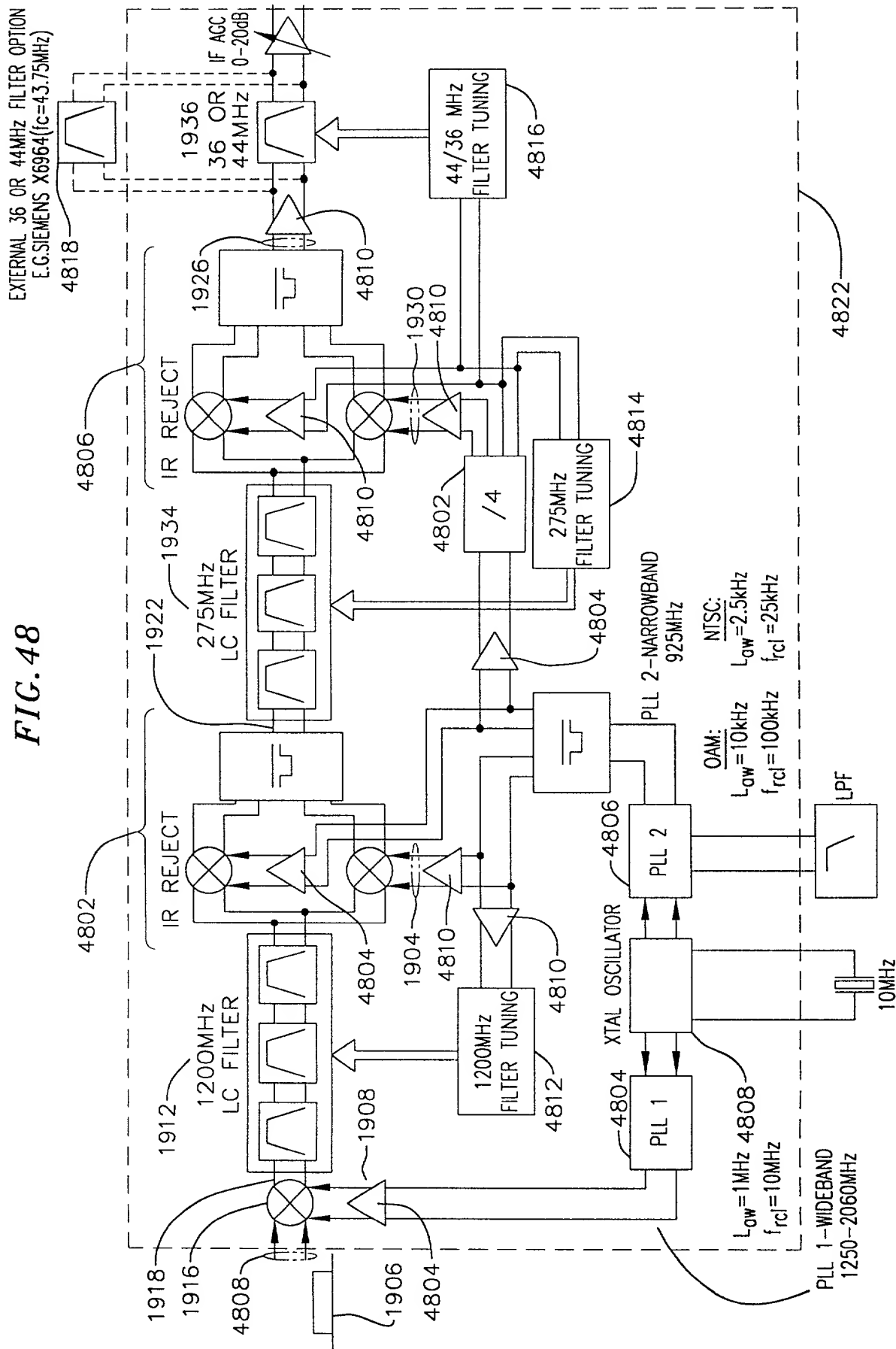


FIG. 49

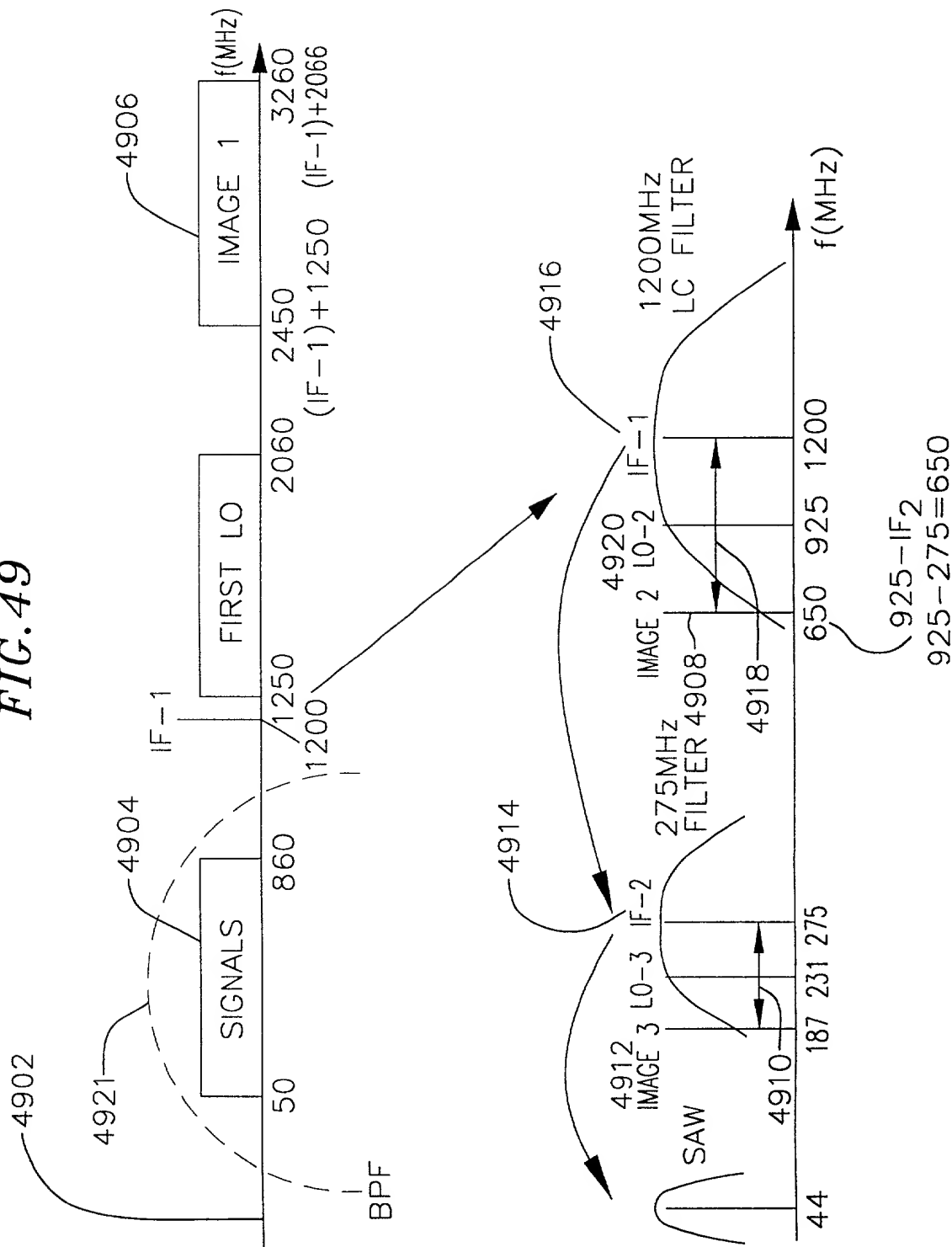
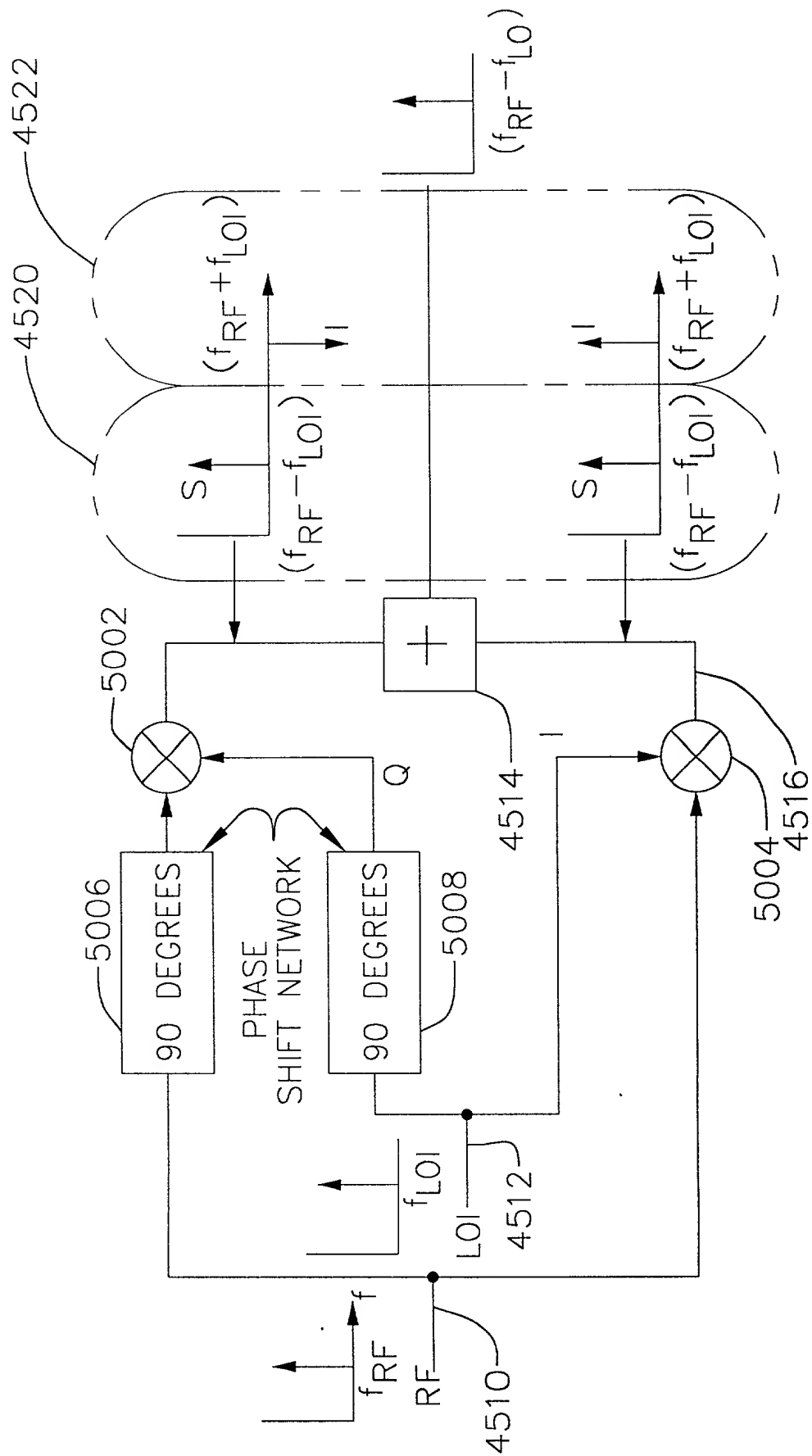
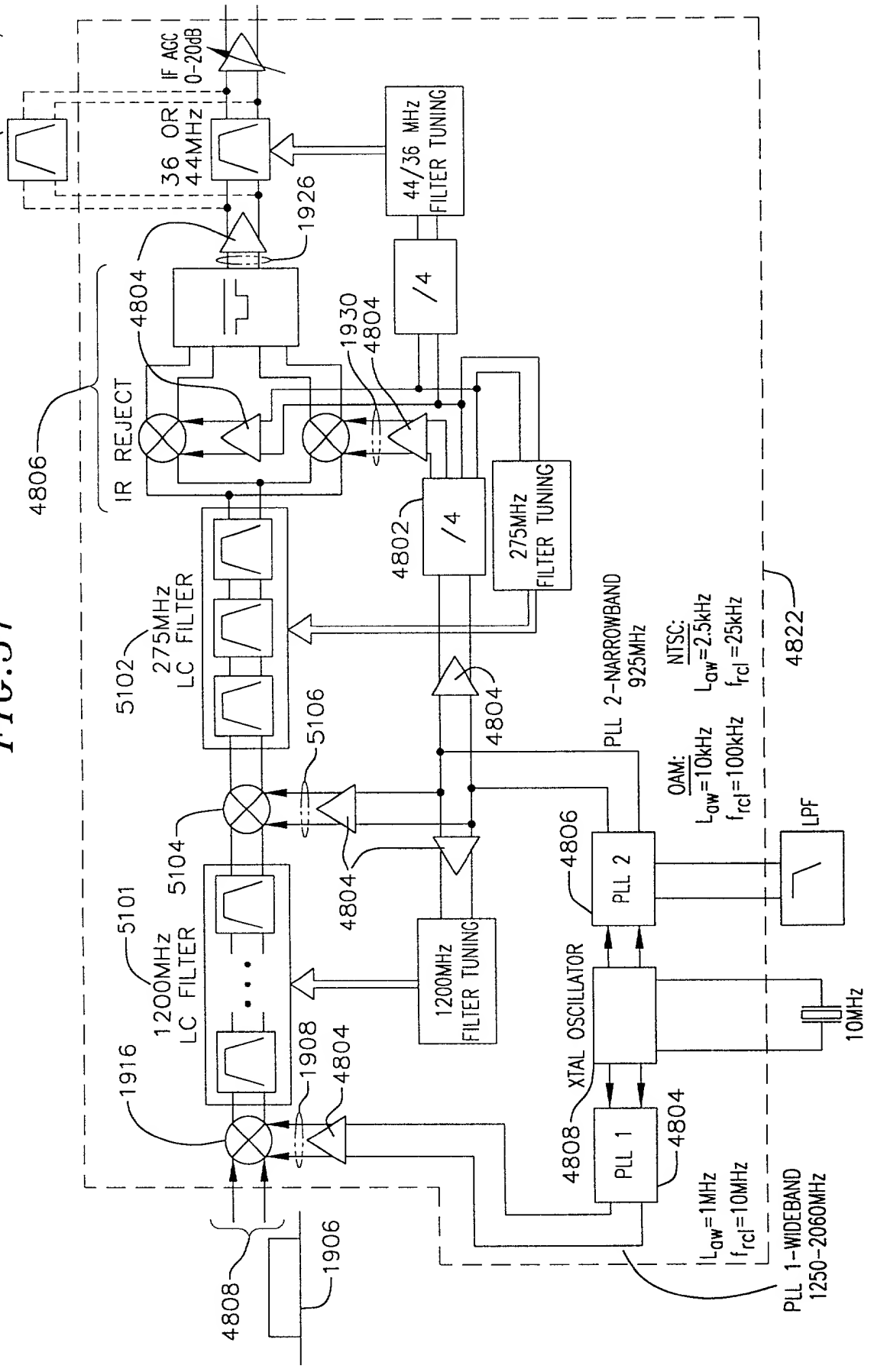


FIG. 50



EXTERNAL 36 OR 44MHz FILTER OPTION
E.G. SIEMENS X6964 ($f_c = 43.75\text{MHz}$)

FIG. 51



EXTERNAL 36 OR 44MHz FILTER OPTION
E.G. SIEMENS X6964 ($f_c = 43.75\text{MHz}$)

FIG. 52

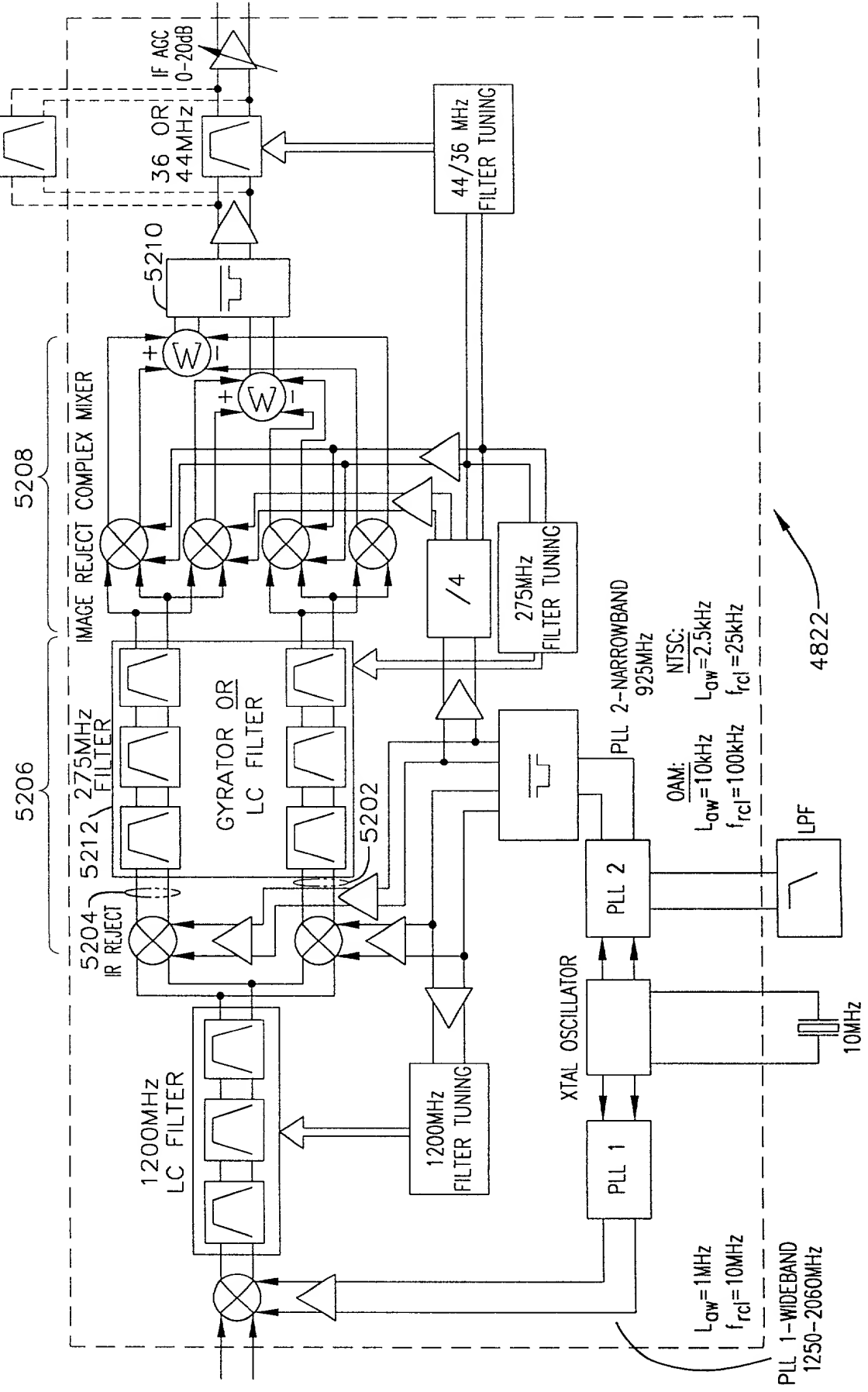


FIG.53
CATV TUNER

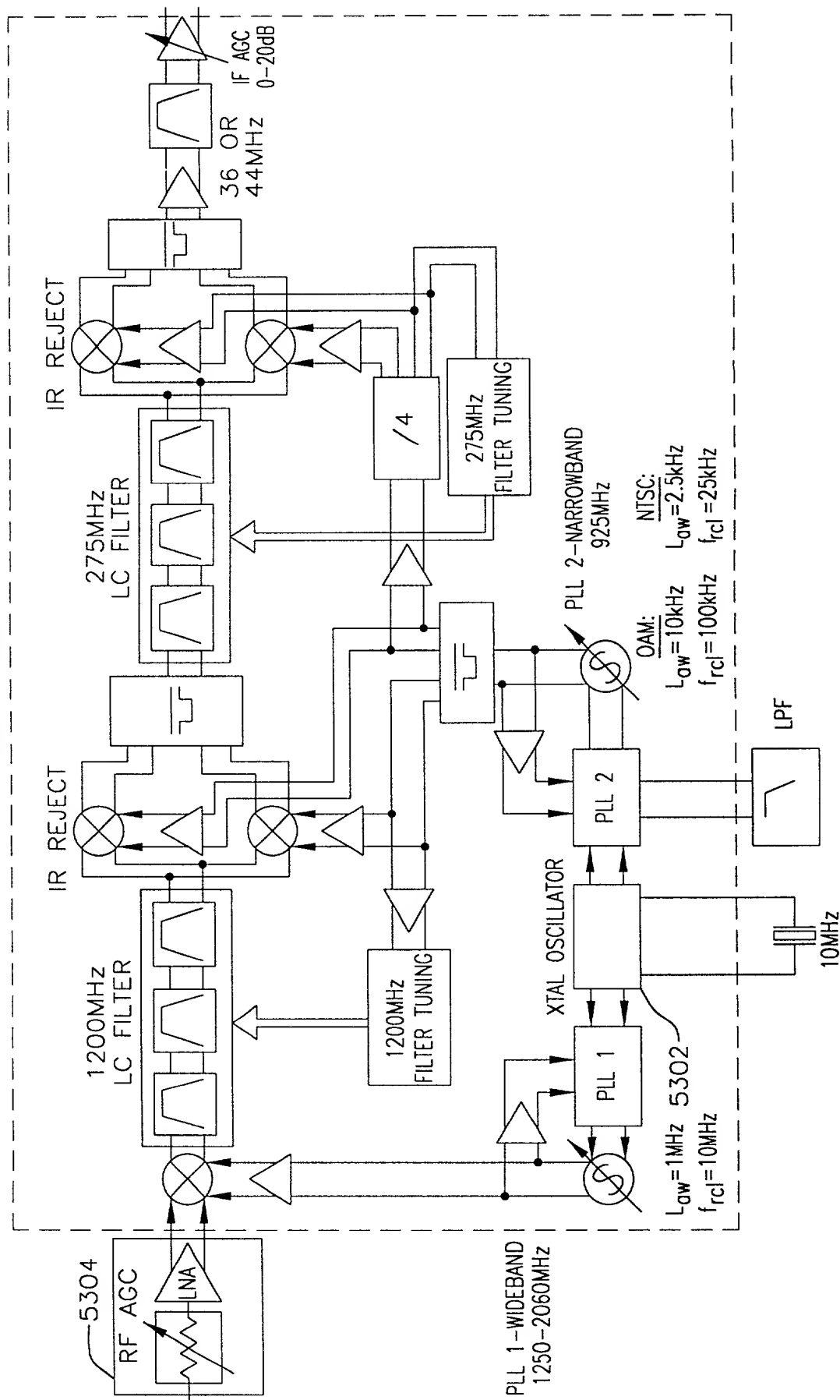
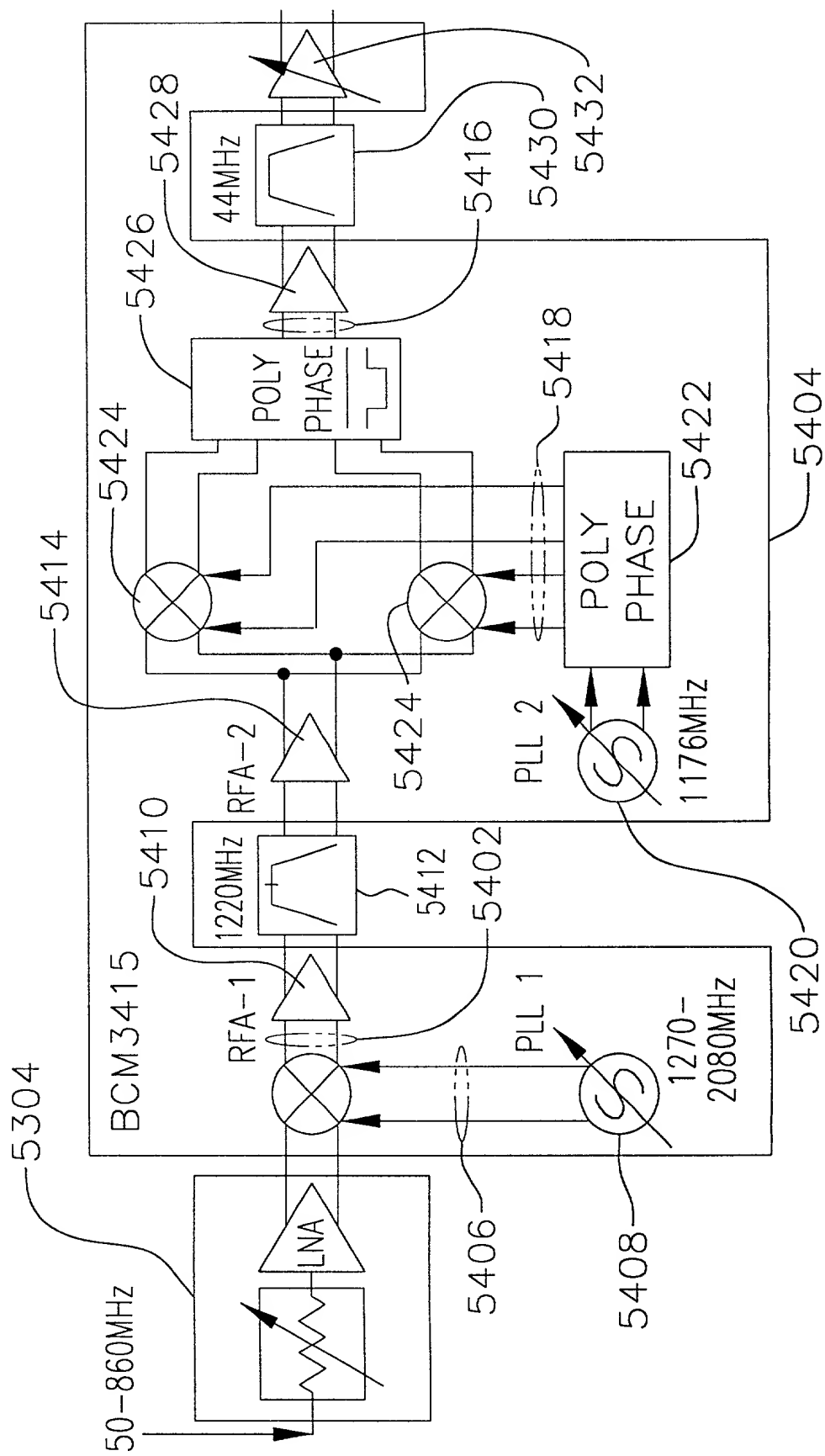
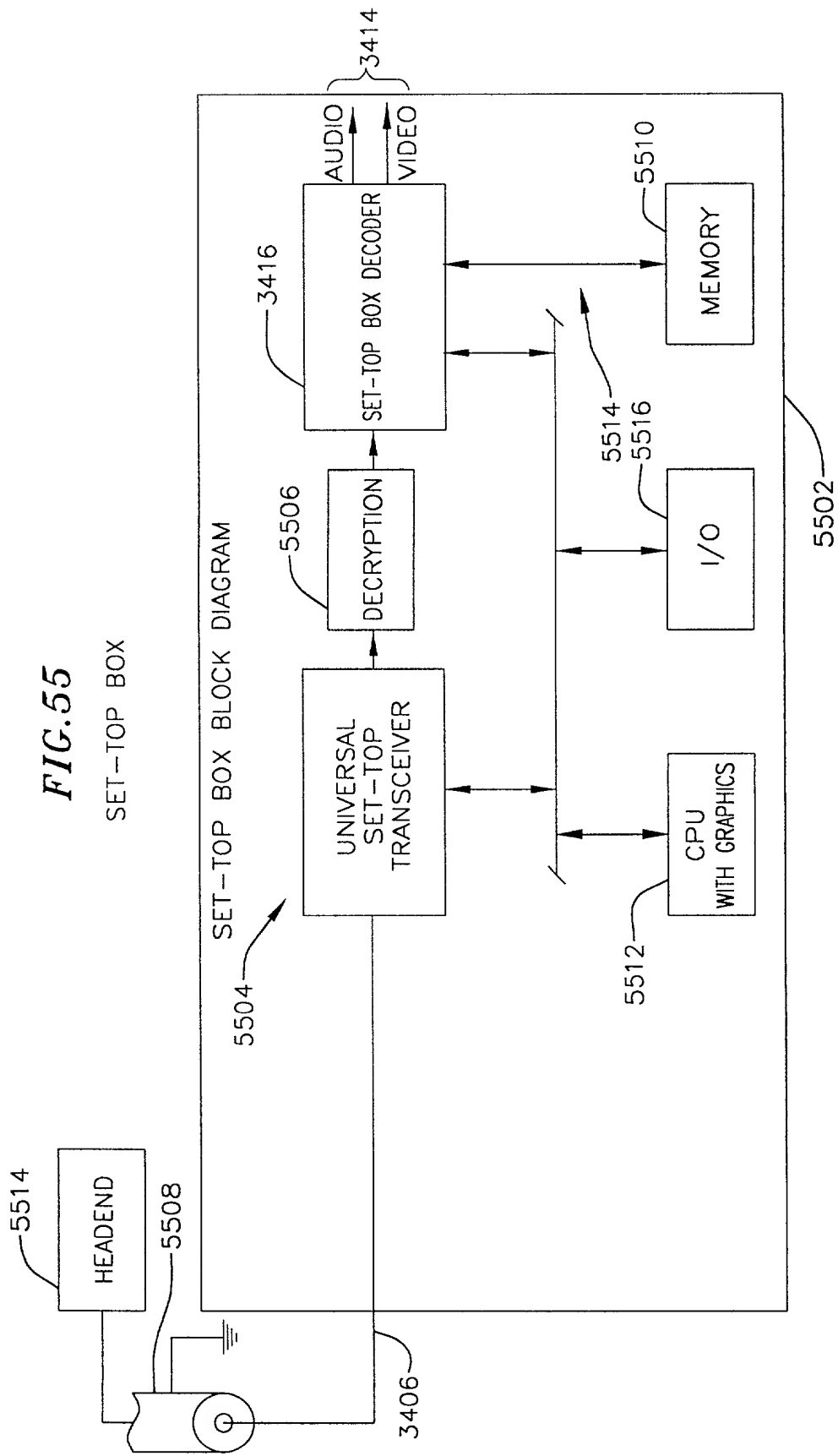


FIG. 54





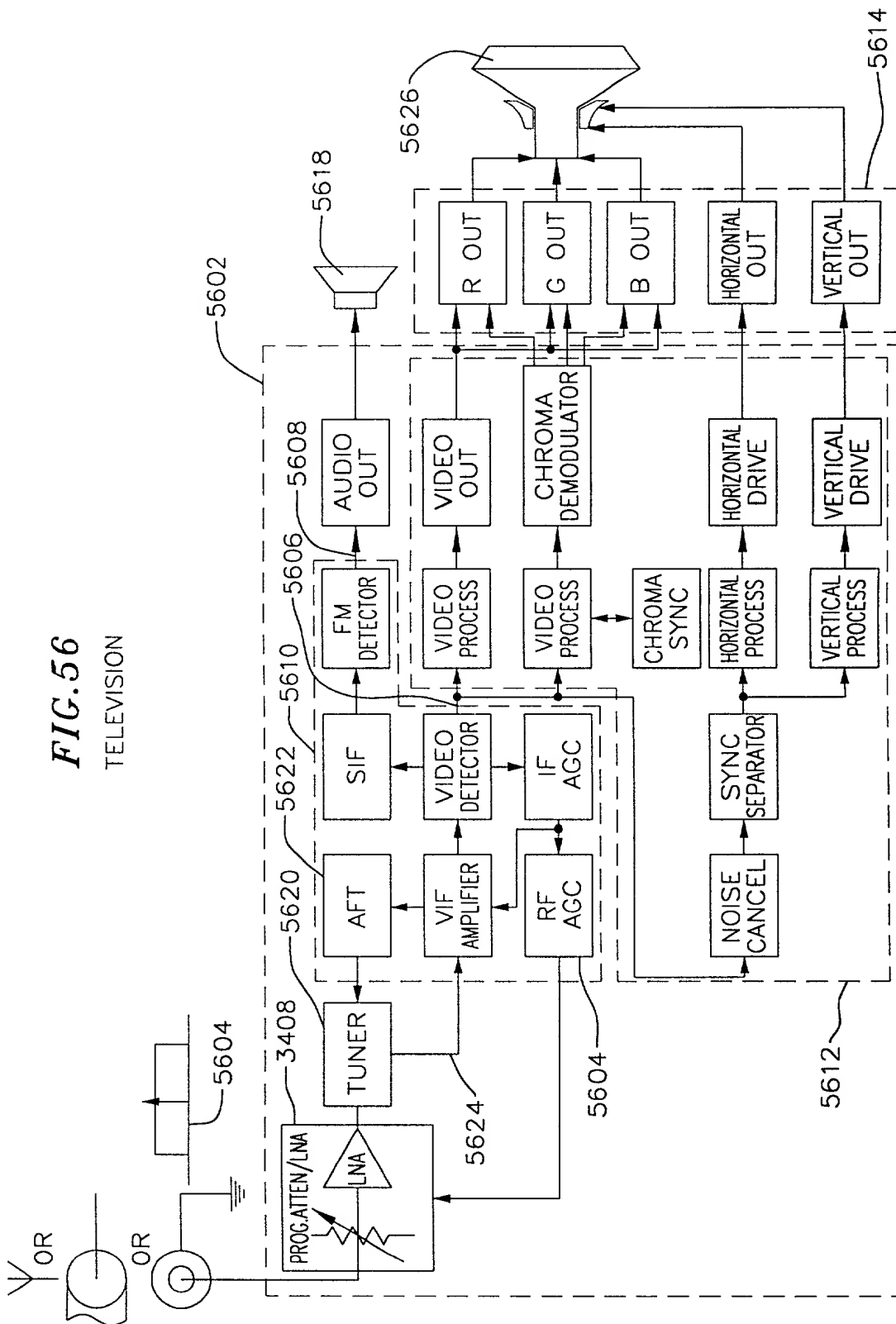


FIG. 57

VCR BLOCK DIAGRAM

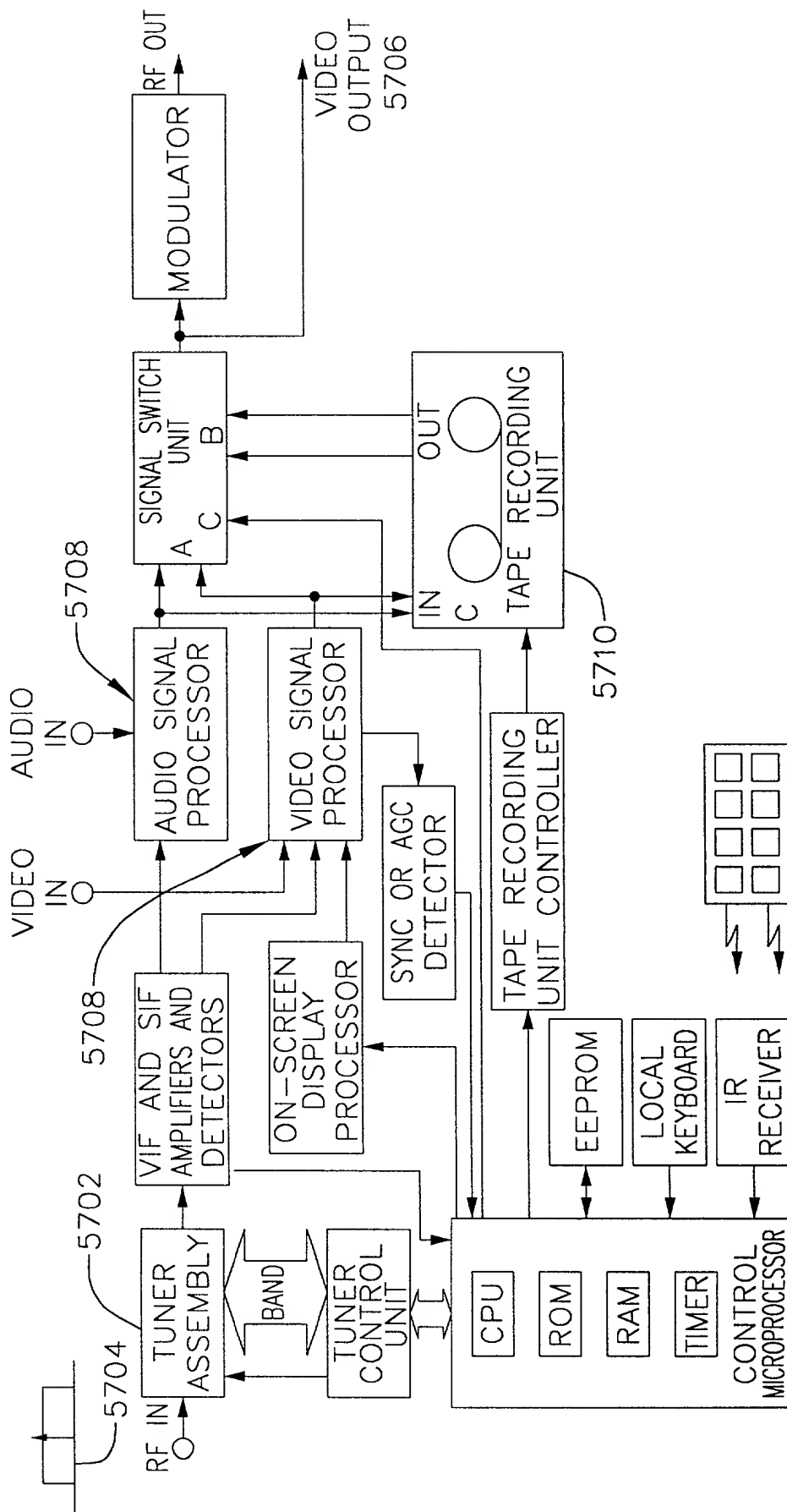


FIG. 58

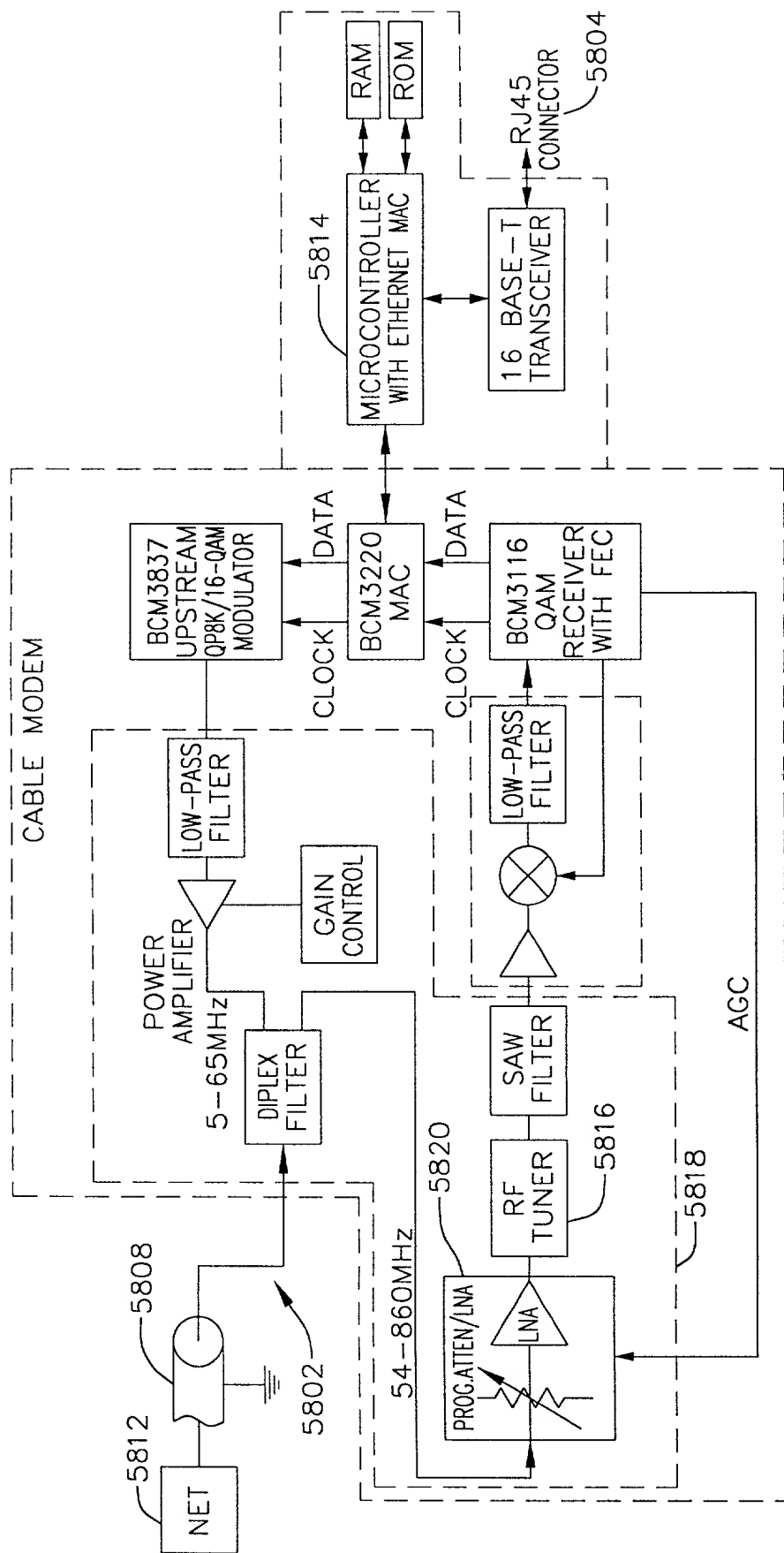


FIG. 59

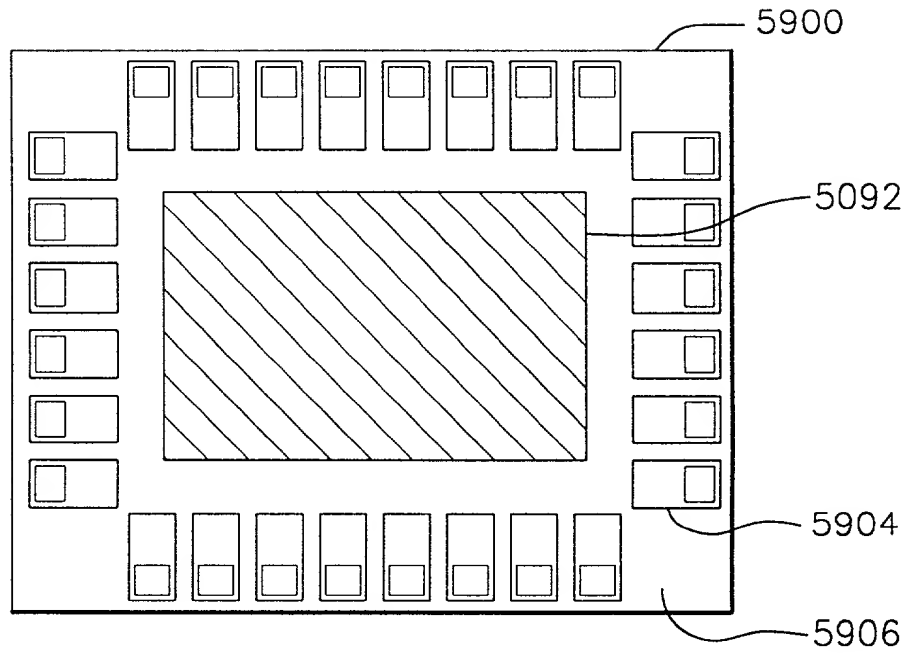


FIG. 60

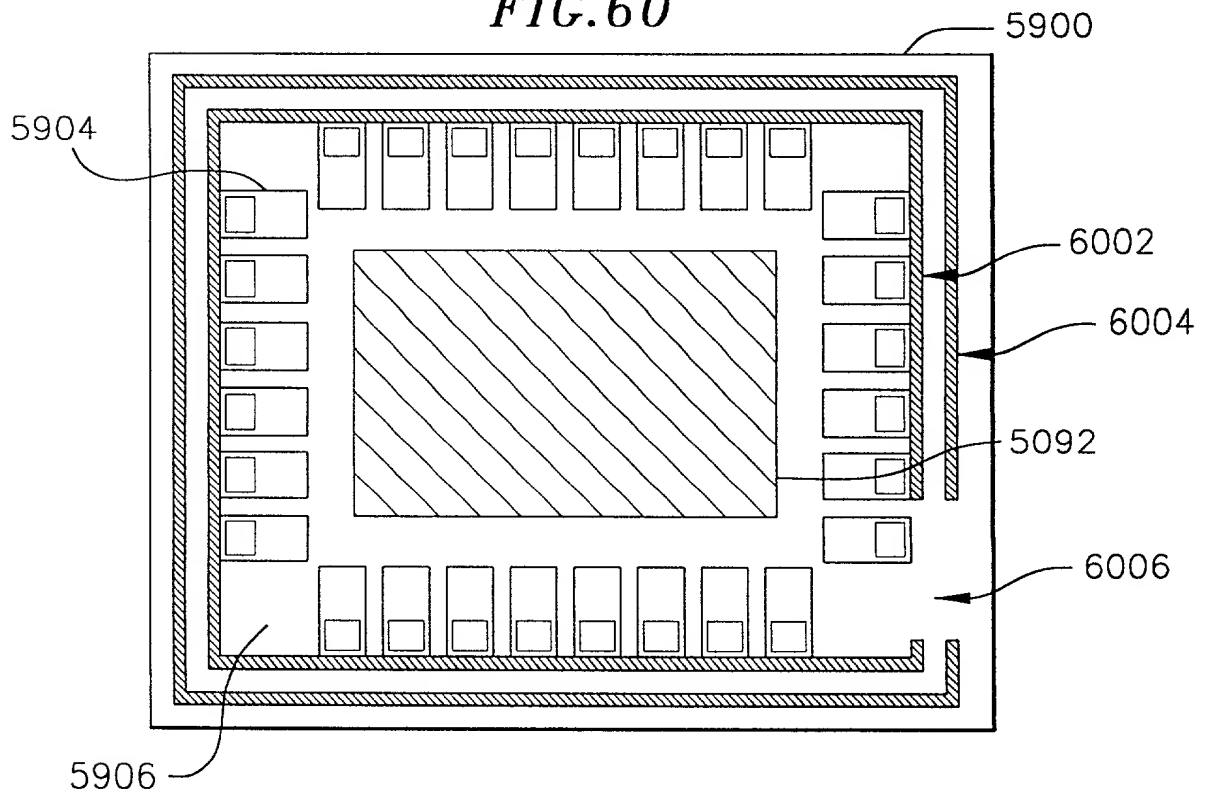


FIG. 61

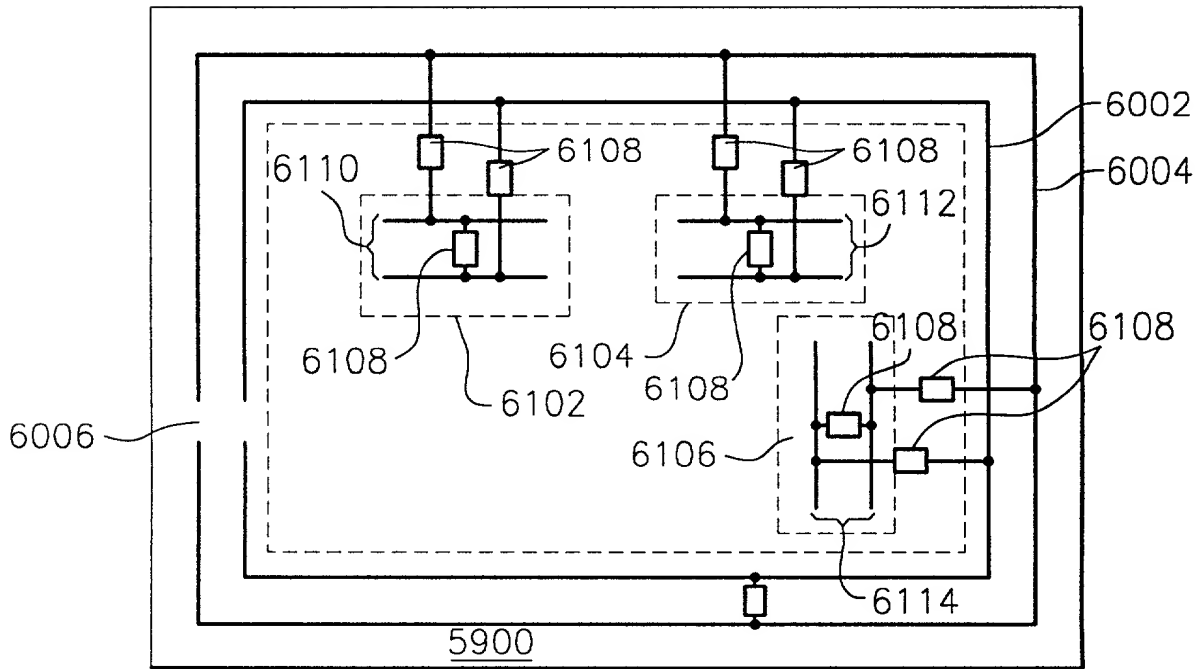


FIG. 62

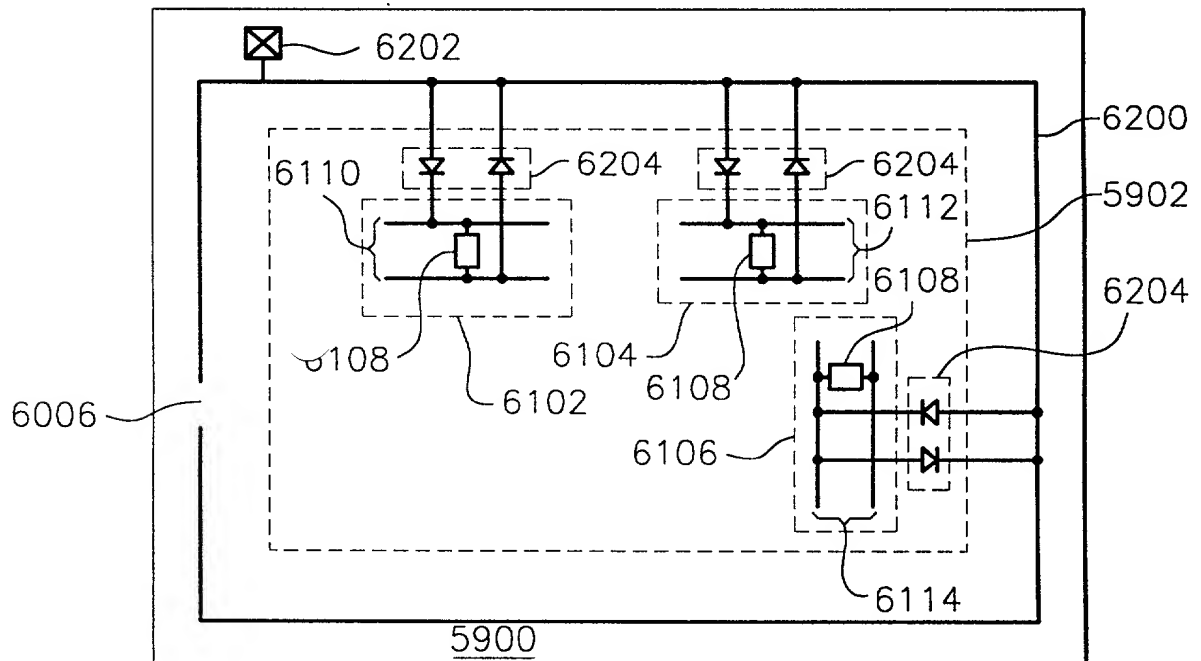


FIG. 63

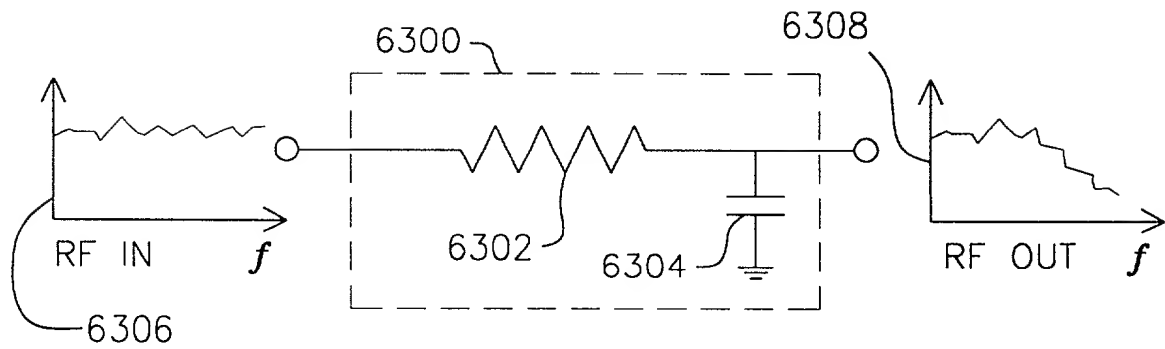


FIG. 64

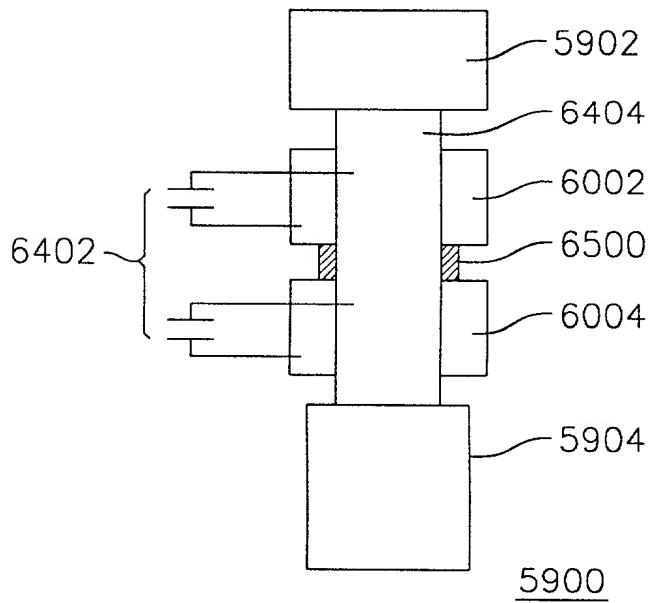
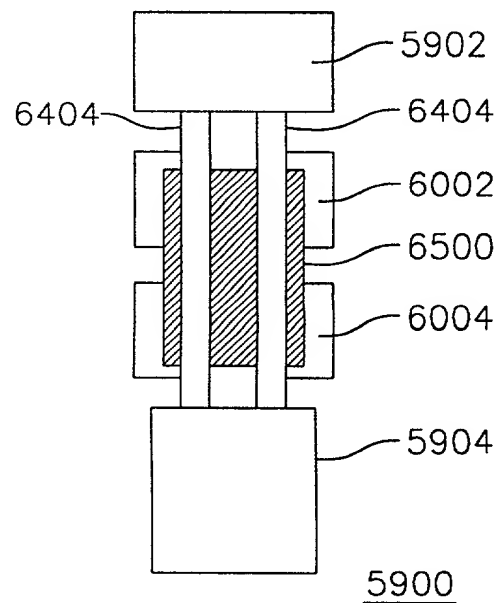


FIG. 65



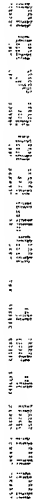
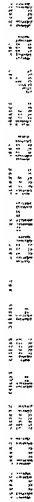


FIG. 68

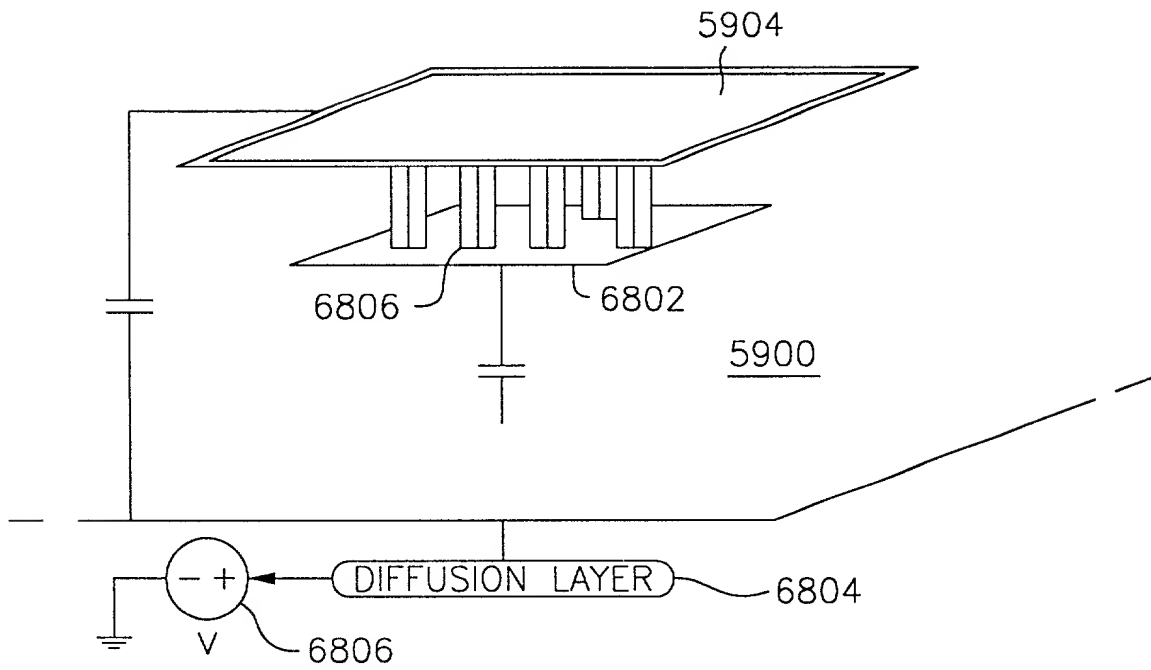


FIG. 69a
PRIOR ART

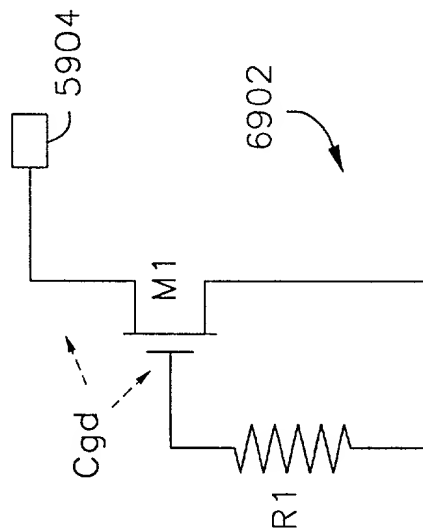


FIG. 69b
PRIOR ART

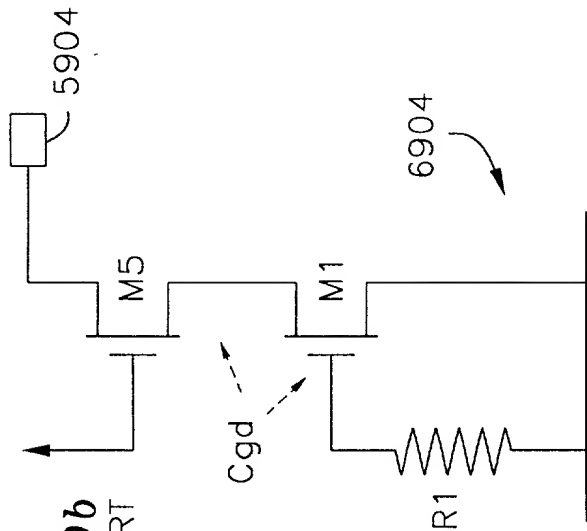


FIG. 69c
PRIOR ART

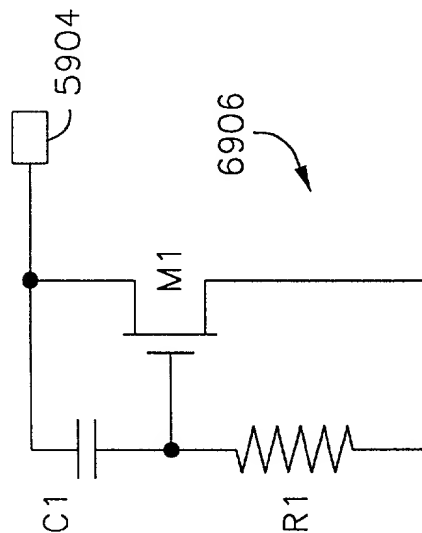


FIG. 69d
PRIOR ART

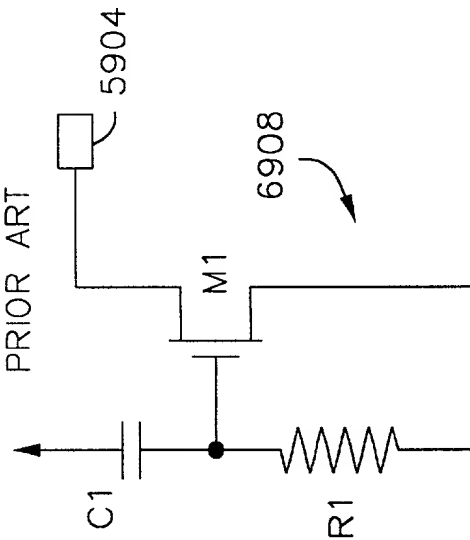


FIG. 69e
PRIOR ART

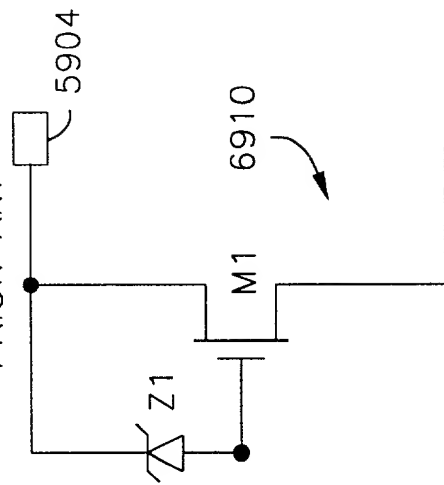


FIG. 70

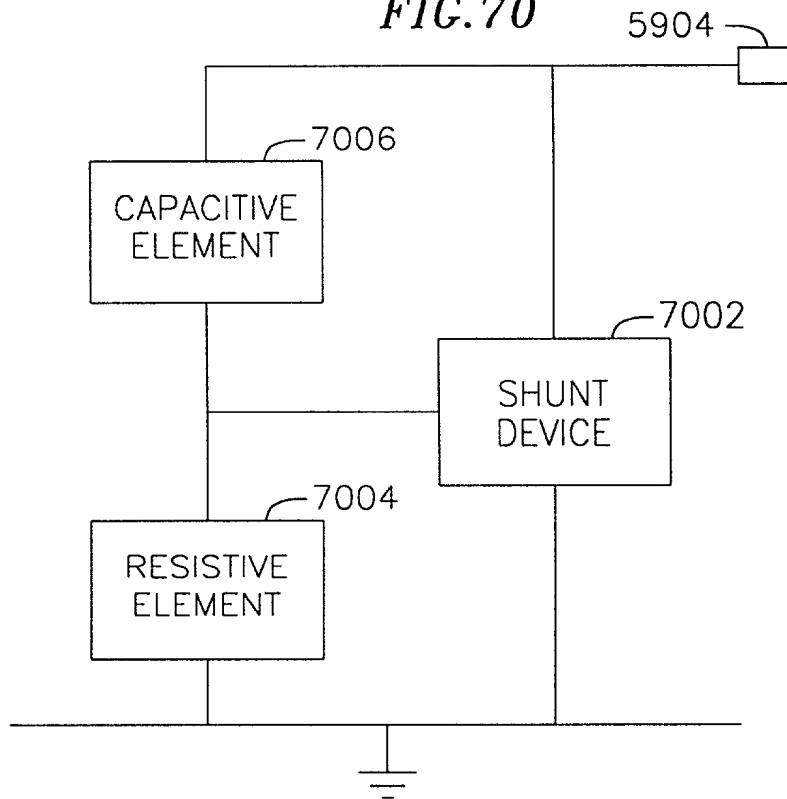


FIG. 71

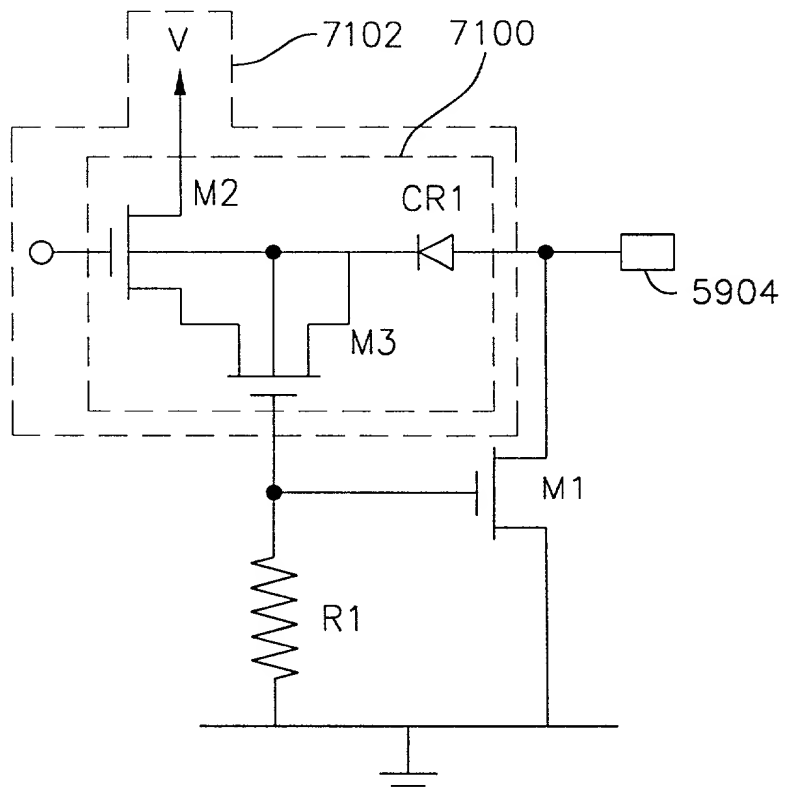


FIG. 72

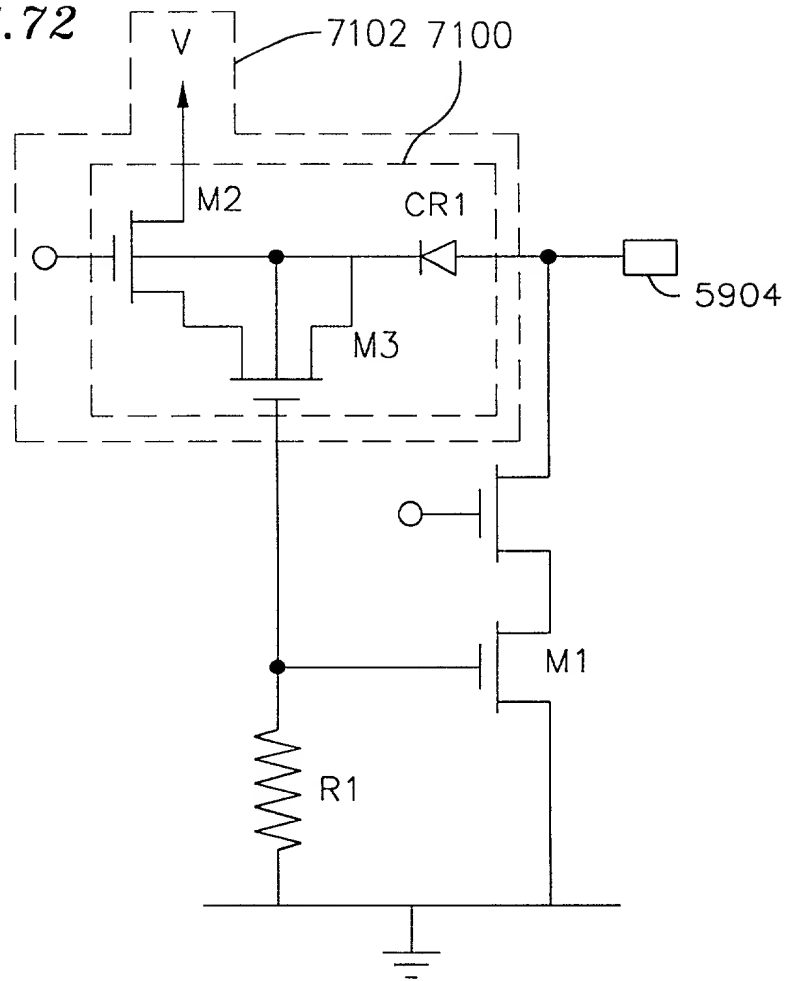


FIG. 73

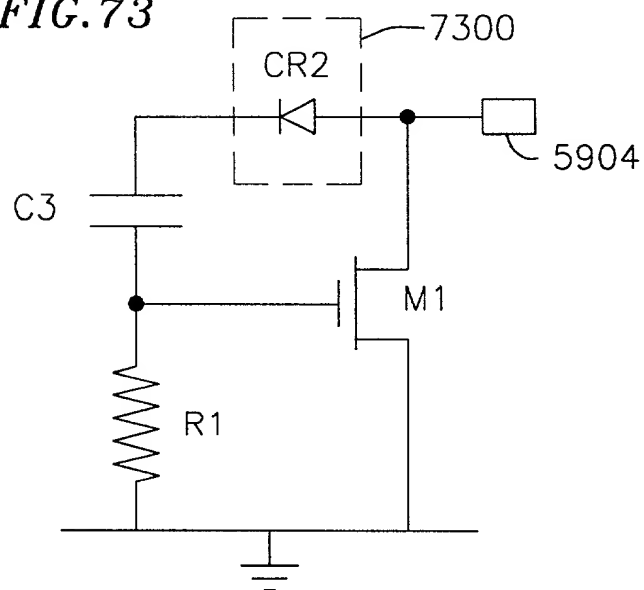
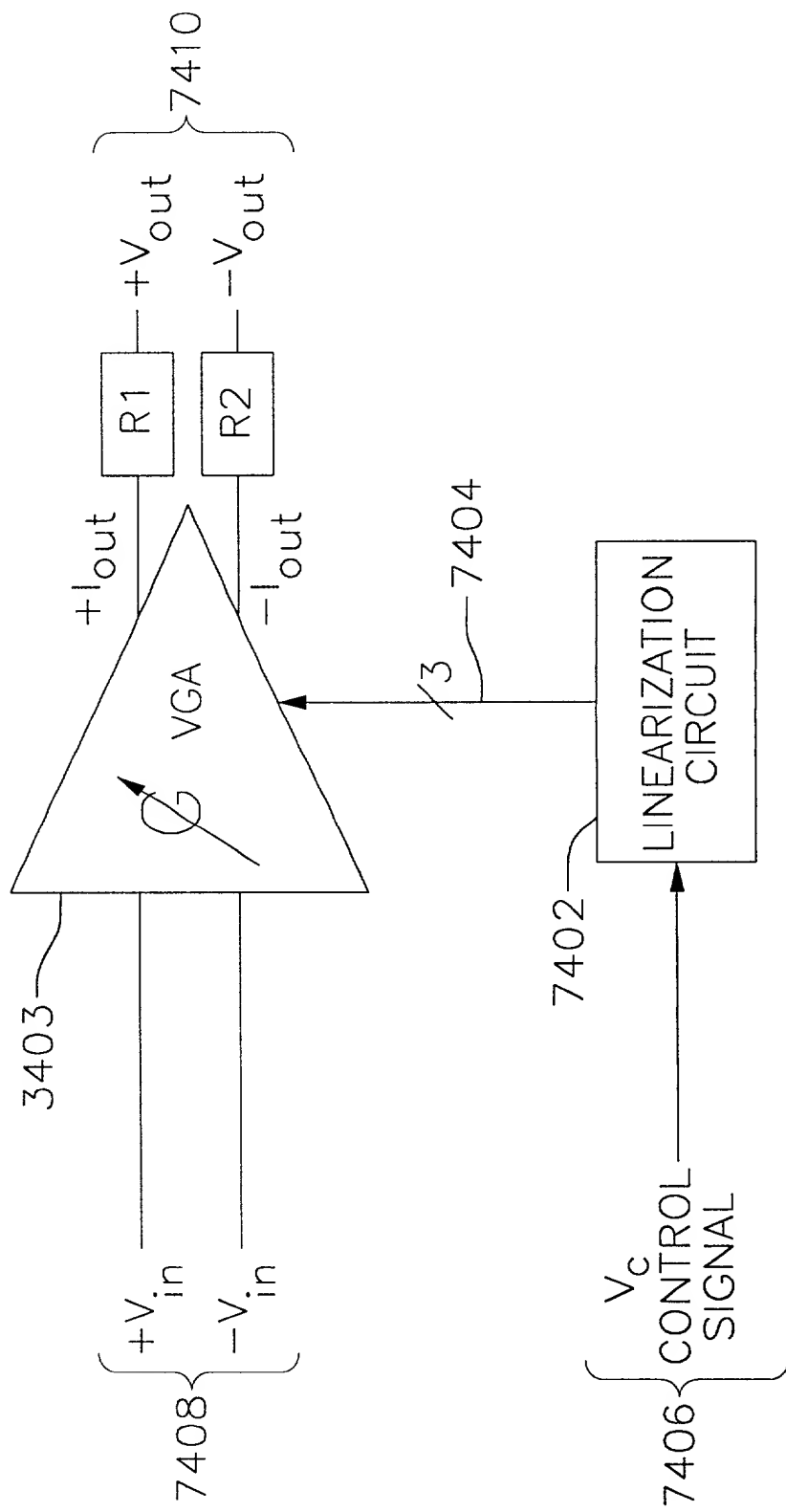


FIG. 74



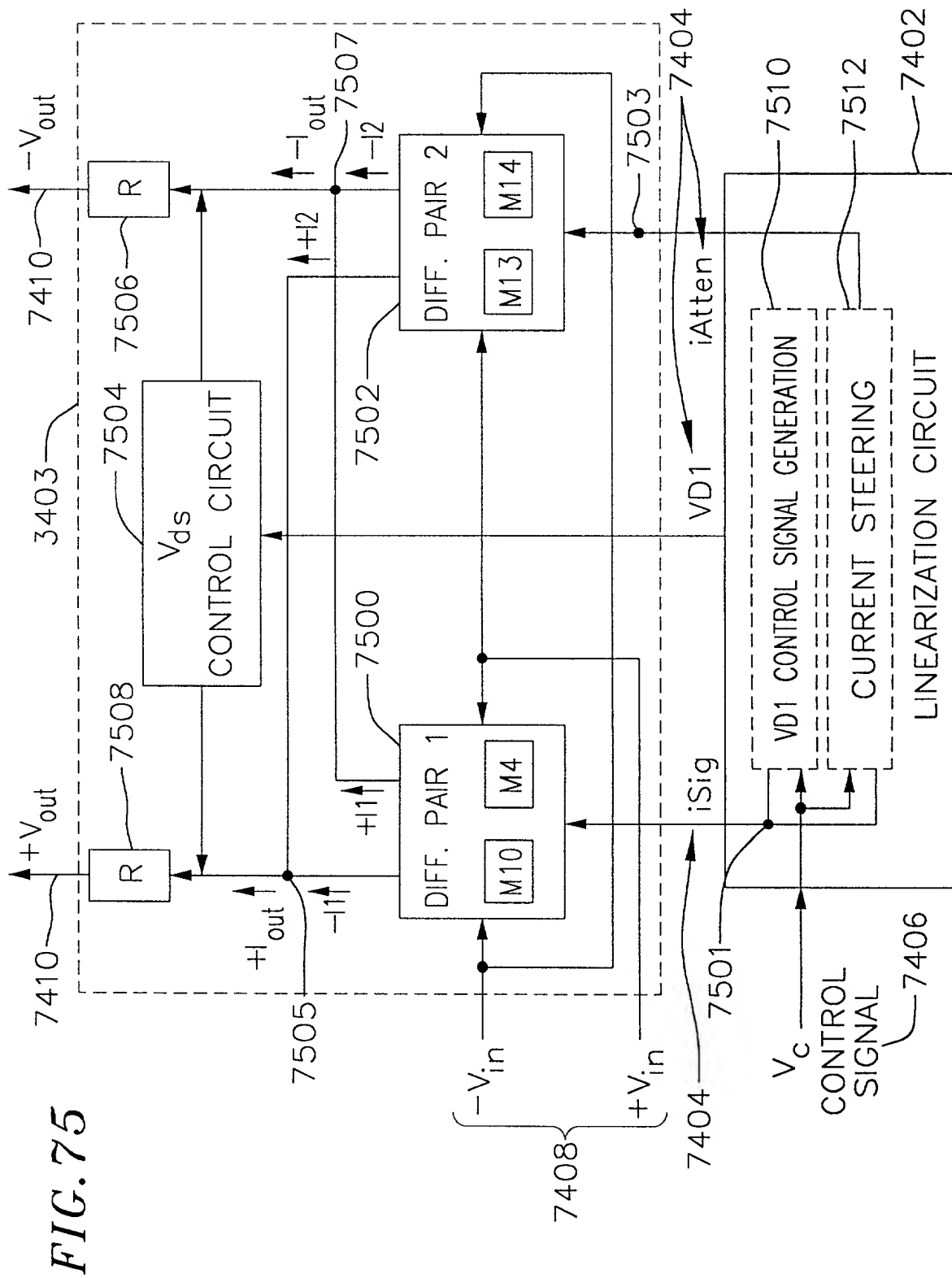


FIG. 76

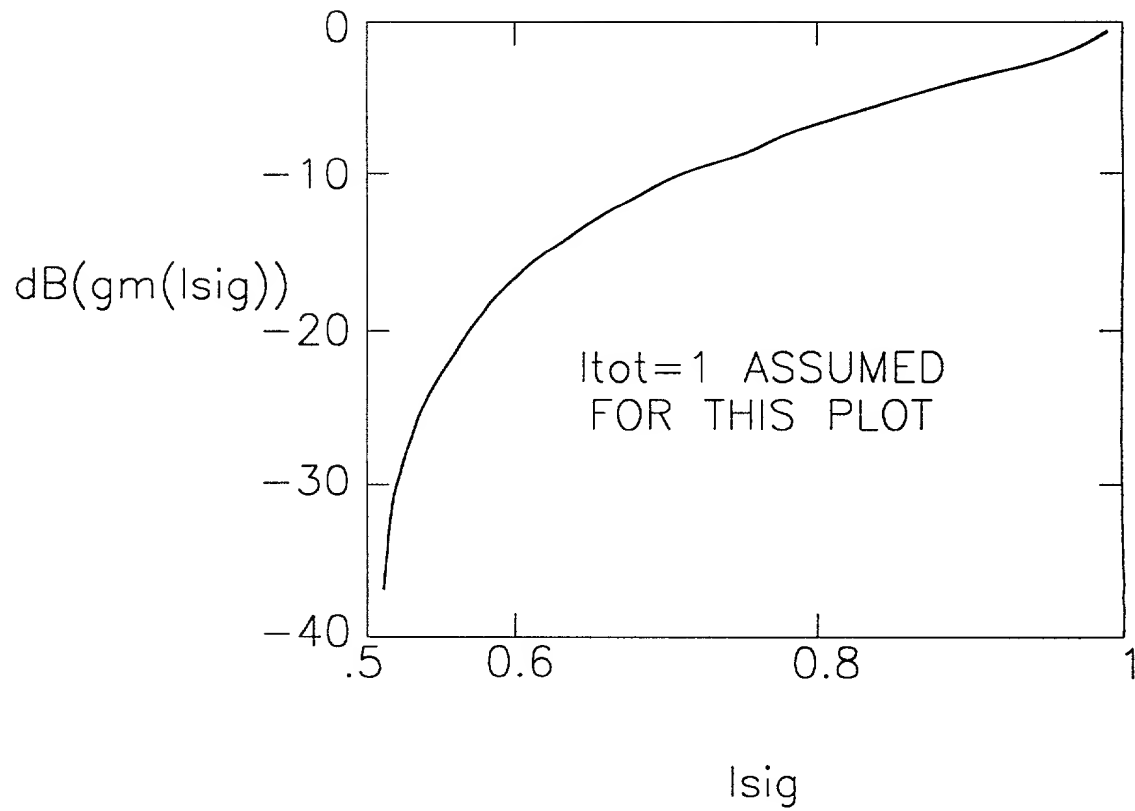


FIG. 77

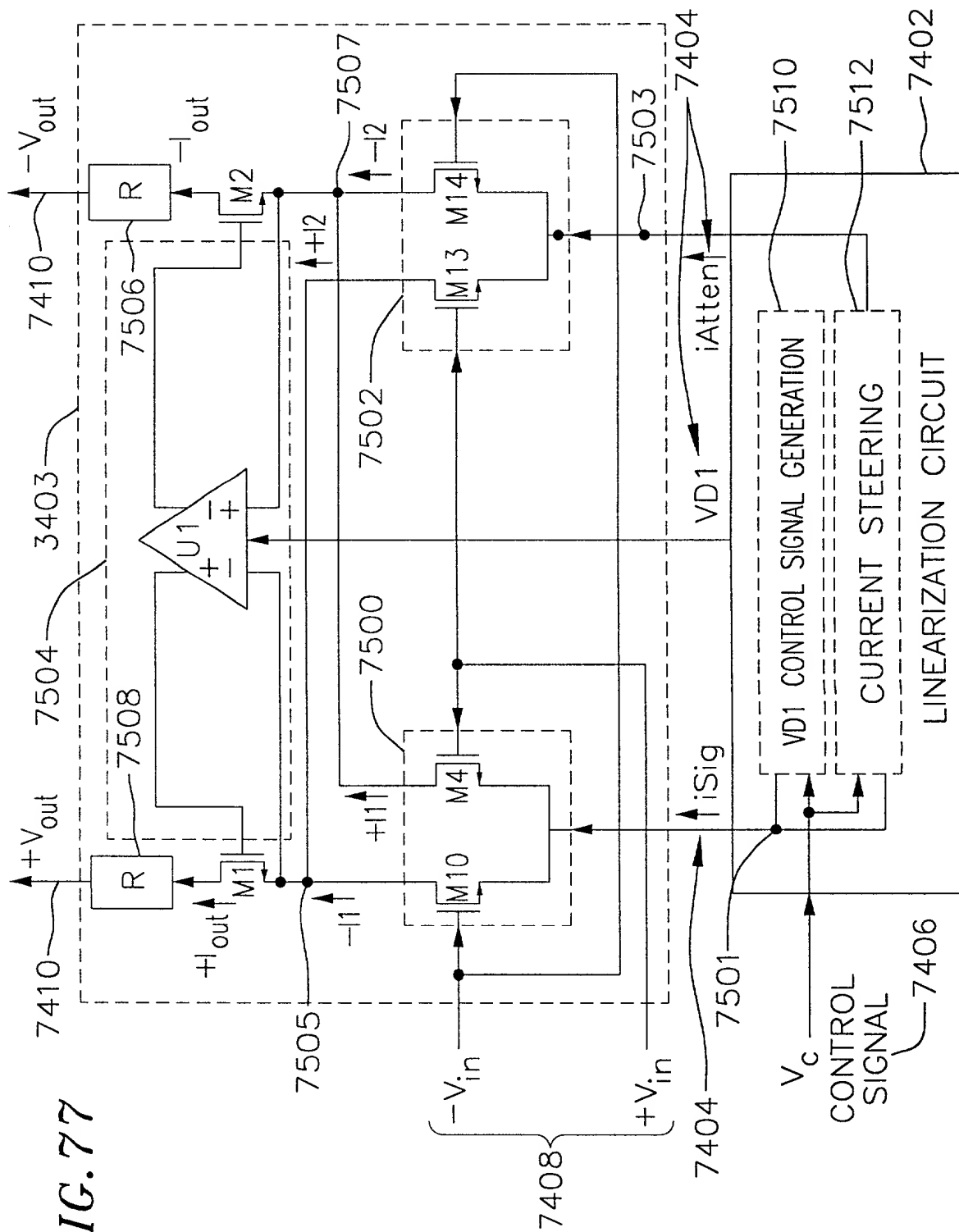


FIG. 78a

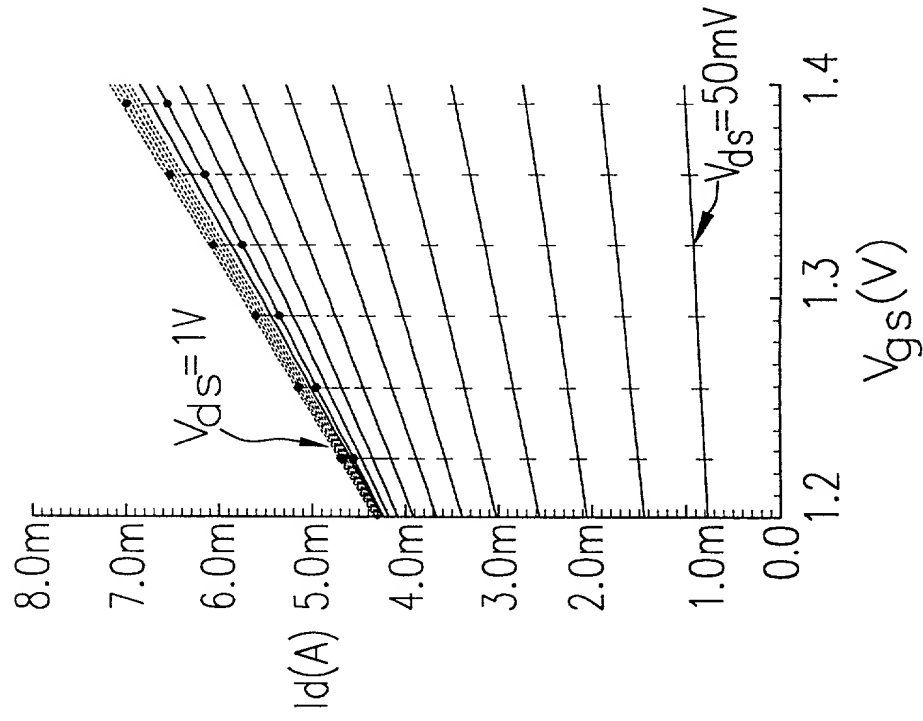


FIG. 78b

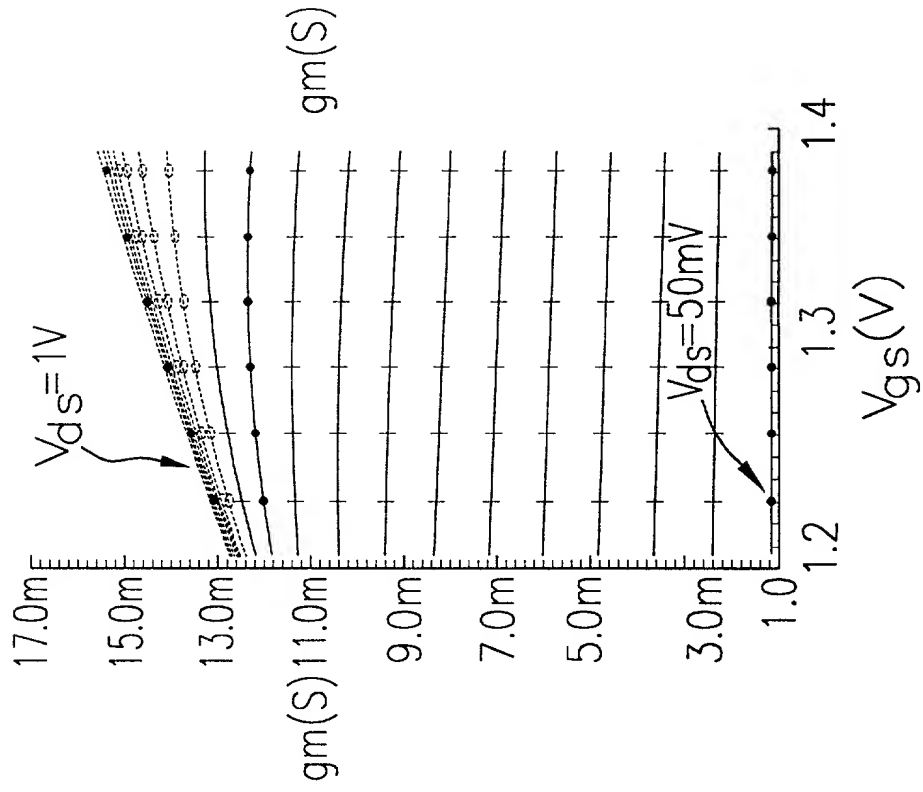
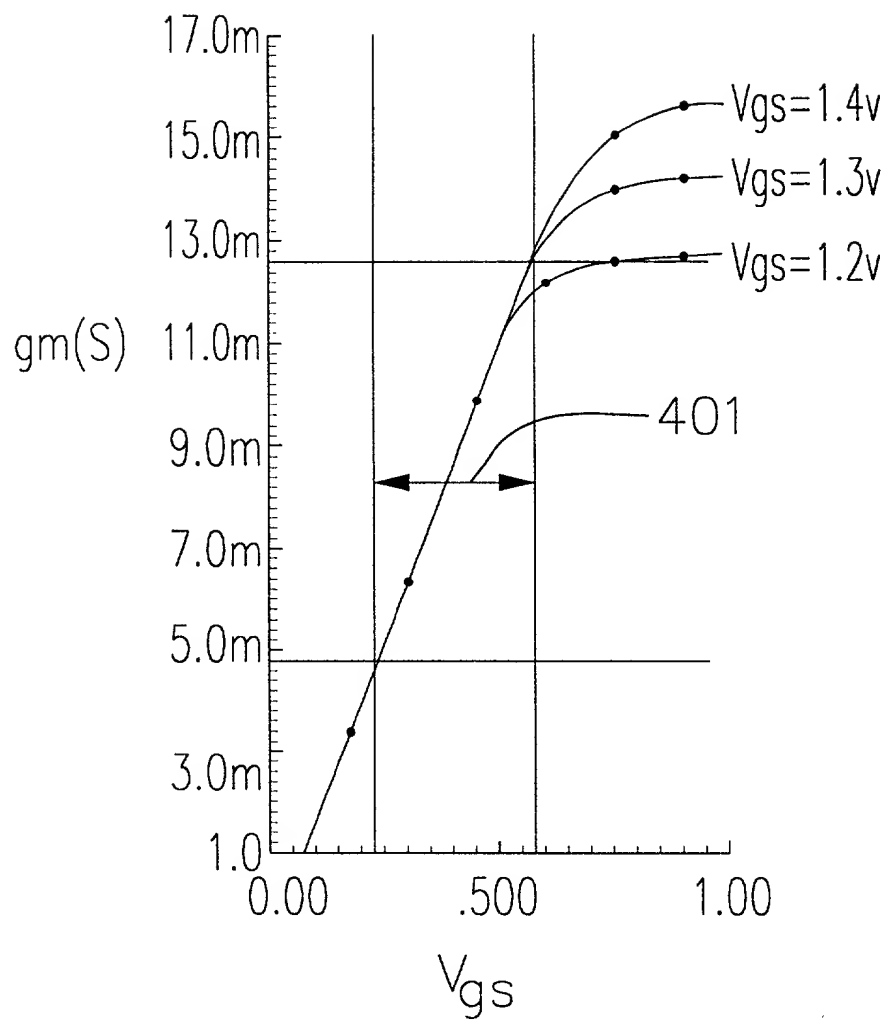
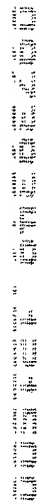
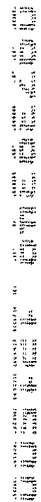


FIG. 78c



[illegible][illegible]

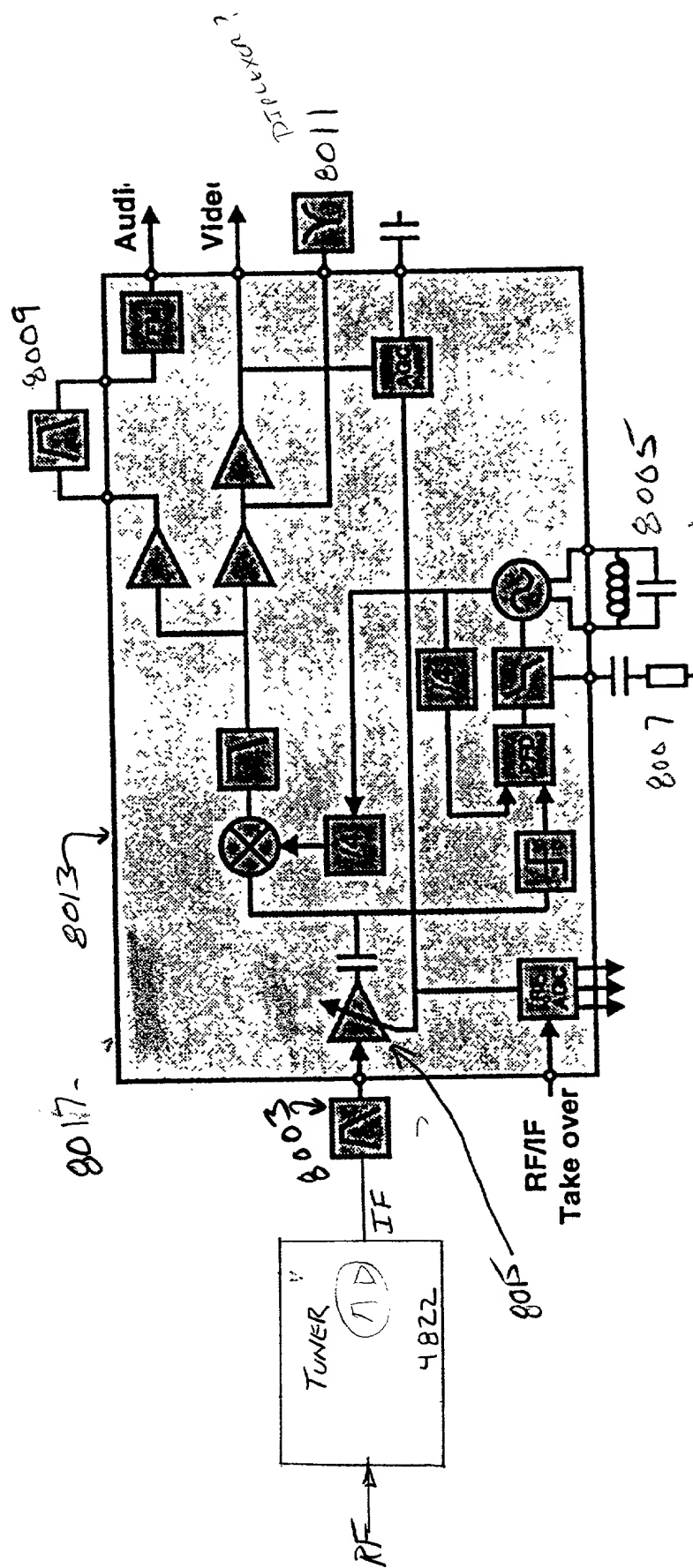
[illegible]

FIG. 1

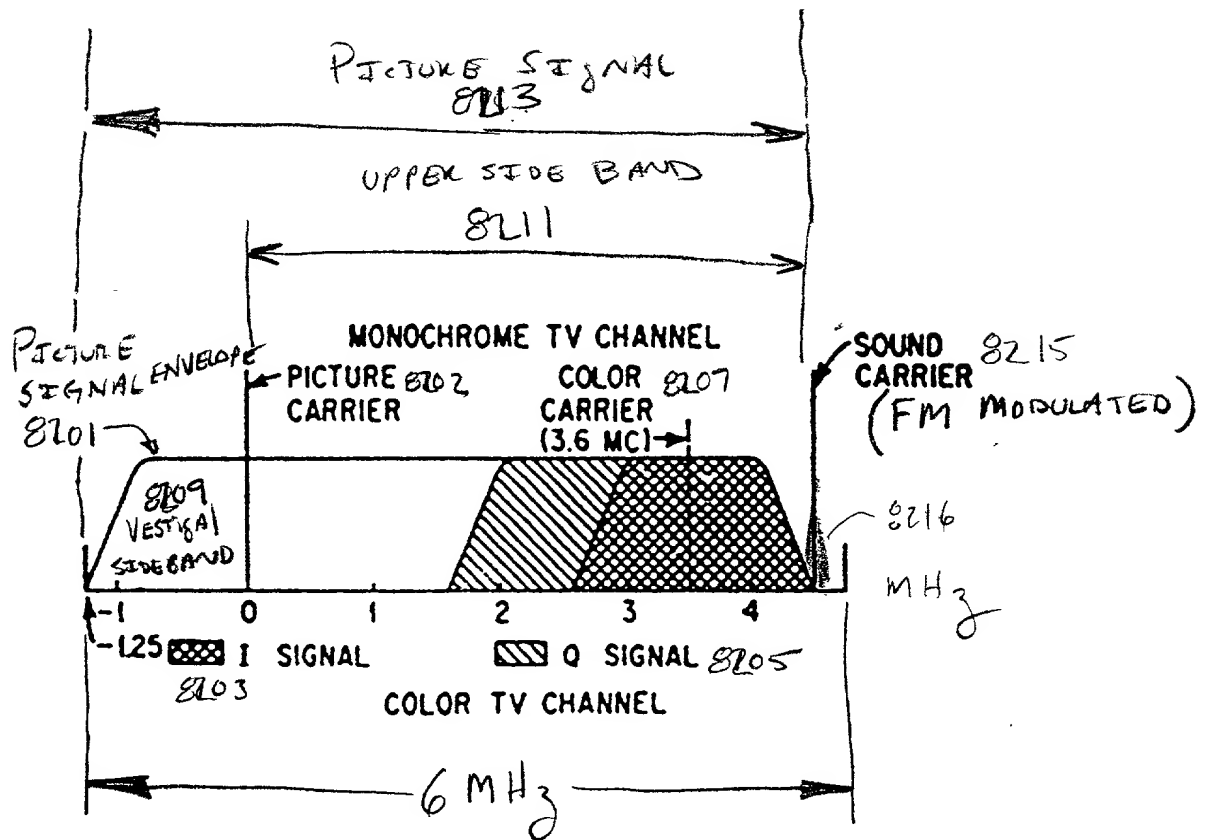


FIG. 82

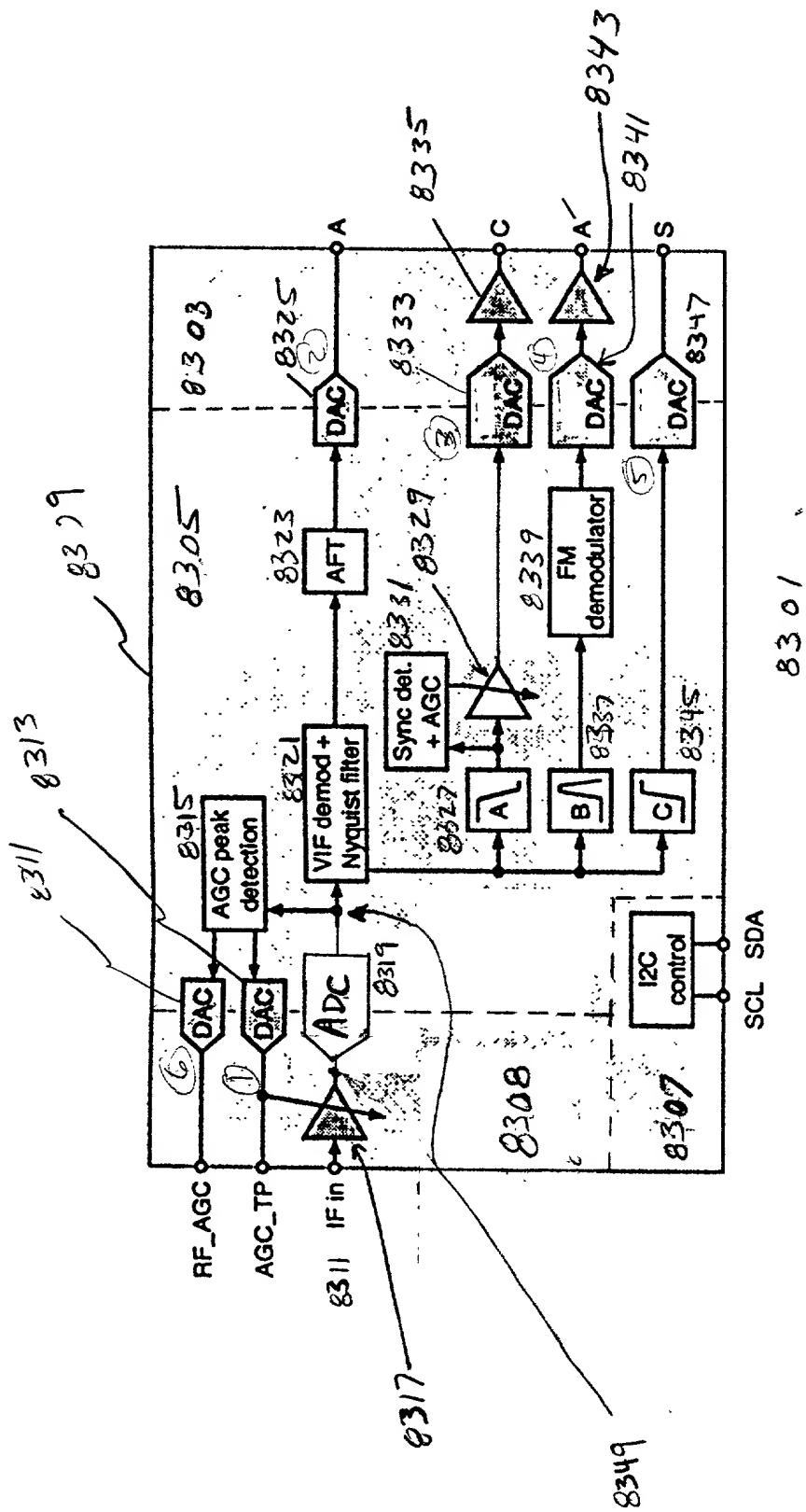
[illegible]

FIG. 3.

FIG. 84a

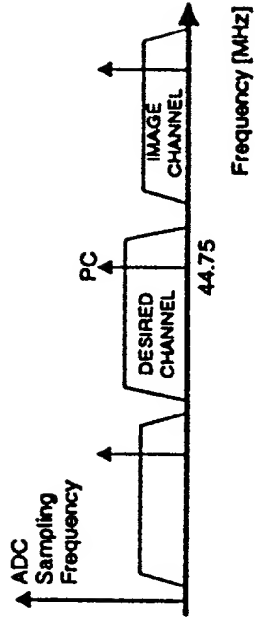


FIG. 84b

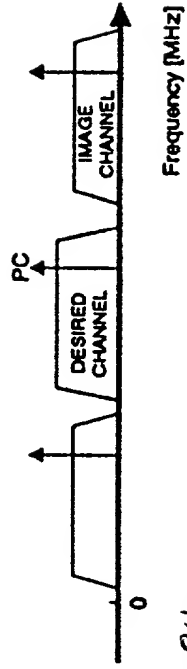


FIG. 84c

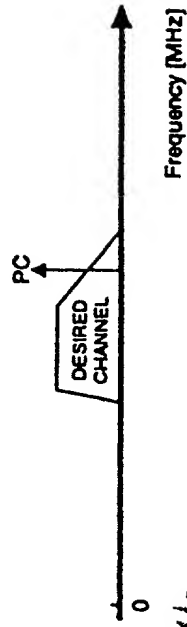


FIG. 84d



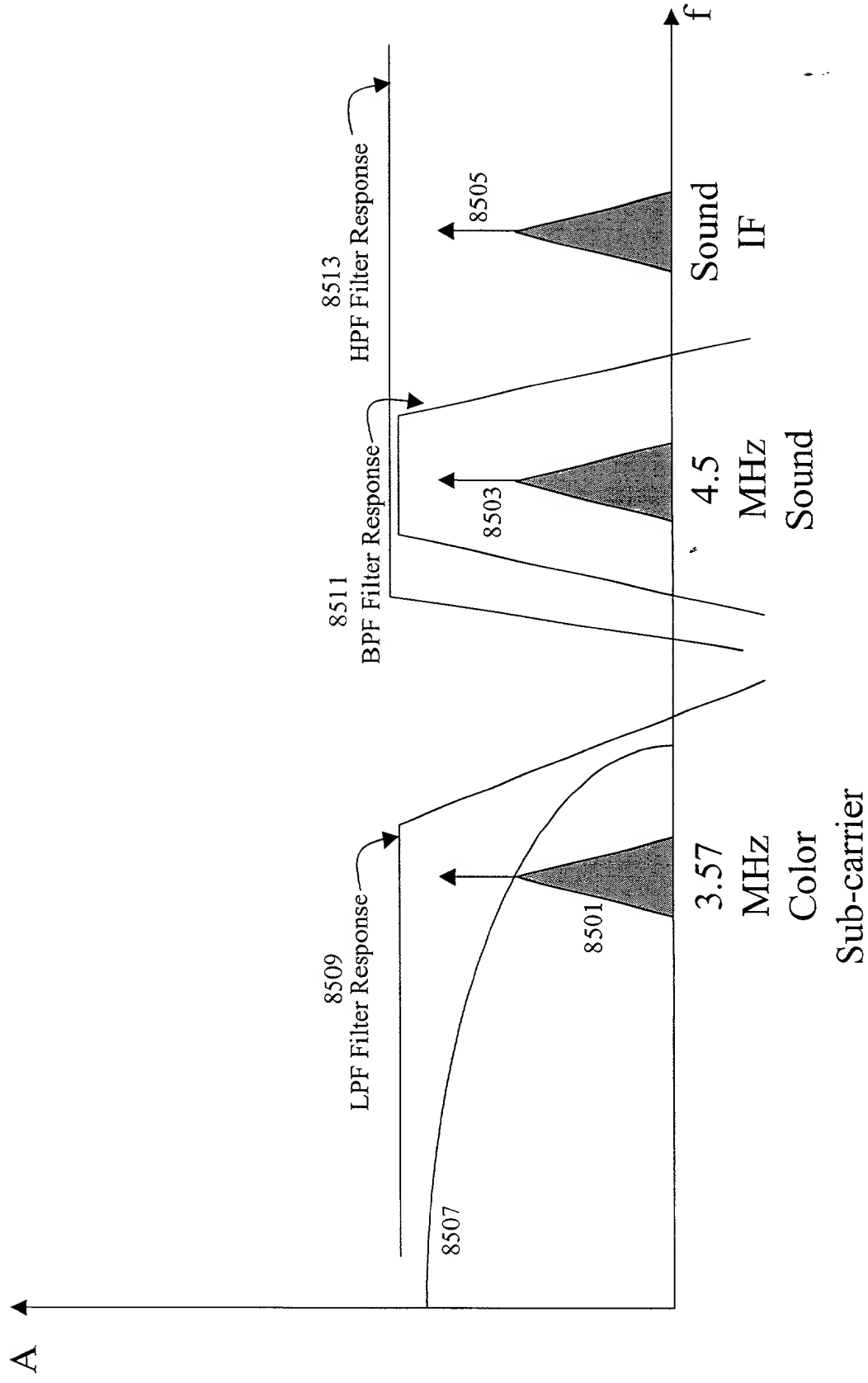


FIG. 85